Error Handling Technologies for QLC-Based Storage System

Wei Lin

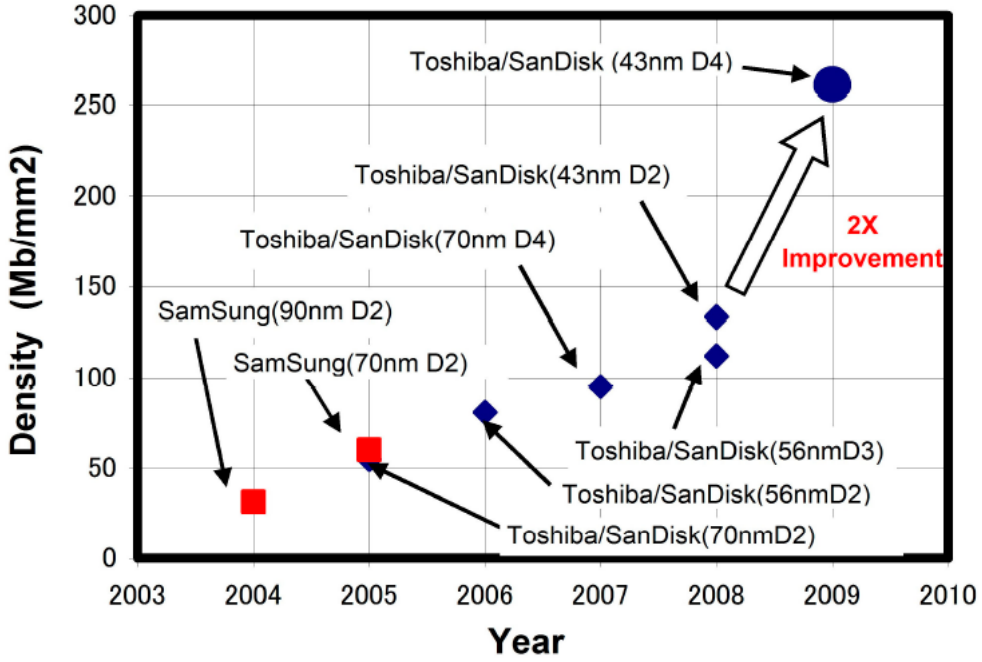
Sr. System Architect, Phison Electronics Corp.

wei_lin@phison.com

Outline

- Introduction to QLC NAND
- Performance issue of QLC
- Reliability issue of QLC
- Algorithms to improve QLC Performance & Reliability
- Conclusions

Memory-density trend since 2003.



A 120mm2 16Gb 4-MLC NAND Flash Memory with 43nm CMOS Technology, ISSCC, 2009

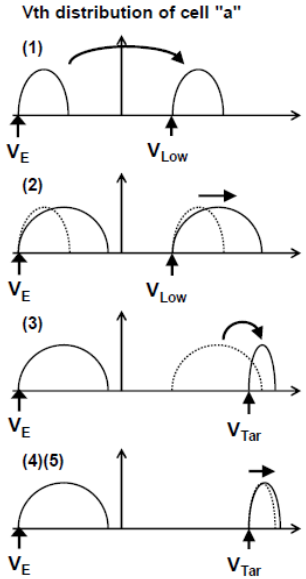
QLC is not a New Idea

ISSCC 2009 / SESSION 13 / FLASH MEMORY / 13.6

13.6 A 5.6MB/s 64Gb 4b/Cell NAND Flash Memory in 43nm CMOS

C. Trinh[1], N. Shibata[2], T. Nakano[2], M. Ogawa[2], J. Sato[2], Y. Takeyama[2], K. Isobe[2], B. Le[1], F. Moogat[1], N. Mokhlesi[1], K. Kozakai[1], P. Hong[1], T. Kamei[1], K. Iwasa[2], J. Nakai[2], T. Shimizu[2], M. Honma[2], S. Sakai[2], T. Kawaai[2], S. Hoshi[2], J. Yuh[1], C. Hsu[1], T. Tseng[1], J. Li[1], J. Hu[1], M. Liu[1], S. Khalid[1], J. Chen[1], M. Watanabe[1], H. Lin[1], J. Yang[1], K. McKay[1], K. Nguyen[1], T. Pham[1], Y. Matsuda[2], K. Nakamura[2], K. Kanebako[2], S. Yoshikawa[2], W. Igarashi[2], A. Inoue[2], T. Takahashi[2], Y. Komatsu[2], C. Suzuki[2], K. Kanazawa[2], M. Higashitani[1], S. Lee[1], T. Murai[1], K. Nguyen[1], J. Lan[1], S. Huynh[1], M. Murin[1], M. Shlick[1], M. Lasser[1], R. Cernea[1], M. Mofidi[1], K. Schuegraf[1], K. Quader[1]

[1]SanDisk, Milpitas, CA
[2]Toshiba, Yokohama, Japan



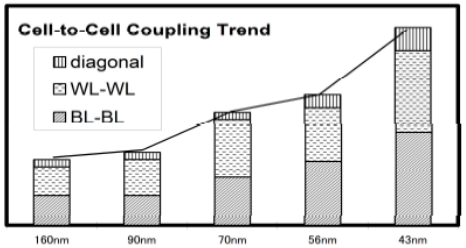
Equation of cell-to-cell interference

C_T = Total Cap of FG
$C_N = 2C_{BL} + C_{WL} + 2C_{diagonal}$
W_{Tar} = Vth distribution width just after program to target level
W_{Low} = Vth distribution width just after program to lower level
DV = Vth shift by cell-to-cell coupling effect when neighbor cell is programmed

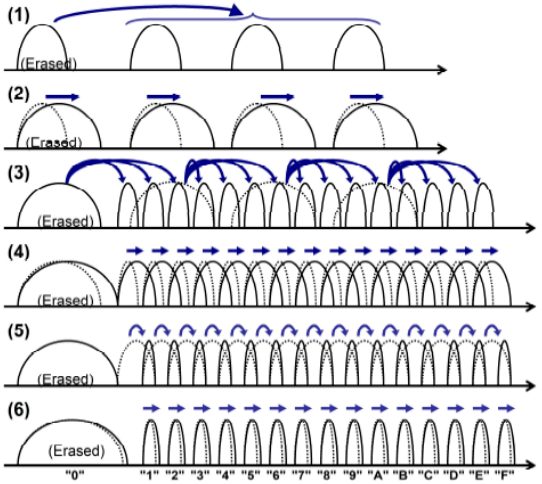
(1) $DV_{Low \to Tar} = (V_{Tar} - V_{Low}) \times \frac{C_N}{C_T}$

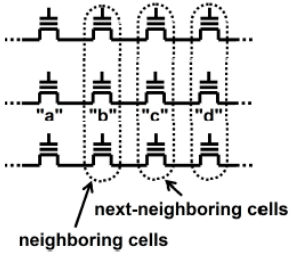
(2) $V_{Tar} + W_{Tar} > V_{Low} + W_{Low} + DV_{E \to Low}$

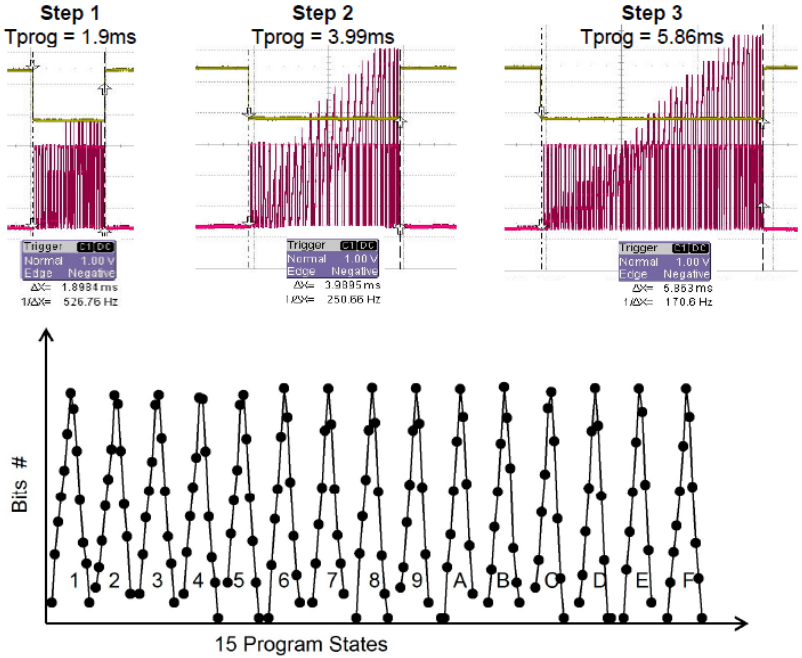
(3) $DV_{E \to Low} = (V_{Low} - V_E) \times \frac{C_N}{C_T}$



Complicated Programing Sequence





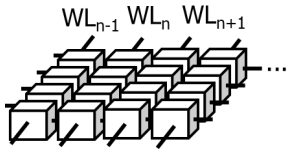
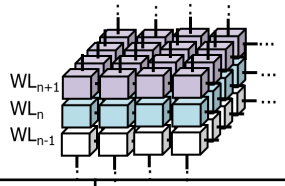
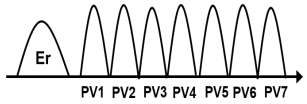
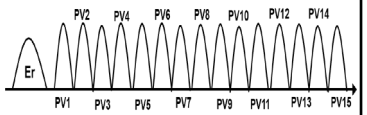


A 120mm2 16Gb 4-MLC NAND Flash Memory with 43nm CMOS Technology, ISSCC, 2009

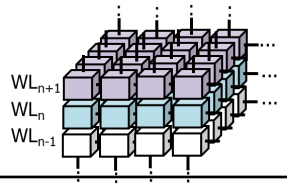
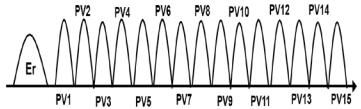
Why Stop 10 years ago?

- Performance
- Reliability

NAND Comparison- QLC mode

	2D-TLC	3D-TLC	3D-QLC
Cell architecture			
Multi-level per cell			
Error behavior (C2CI+Vth window)	Δ	o	x
Program algorithm	Multi-pass	Single-pass	Multi-pass
Performance	Δ	o	x
Reliability (DR/RD…)	Δ	o	x
DPPM issue	-	WL leakage (Program operation)	

Phison's DSPand System Algorithm

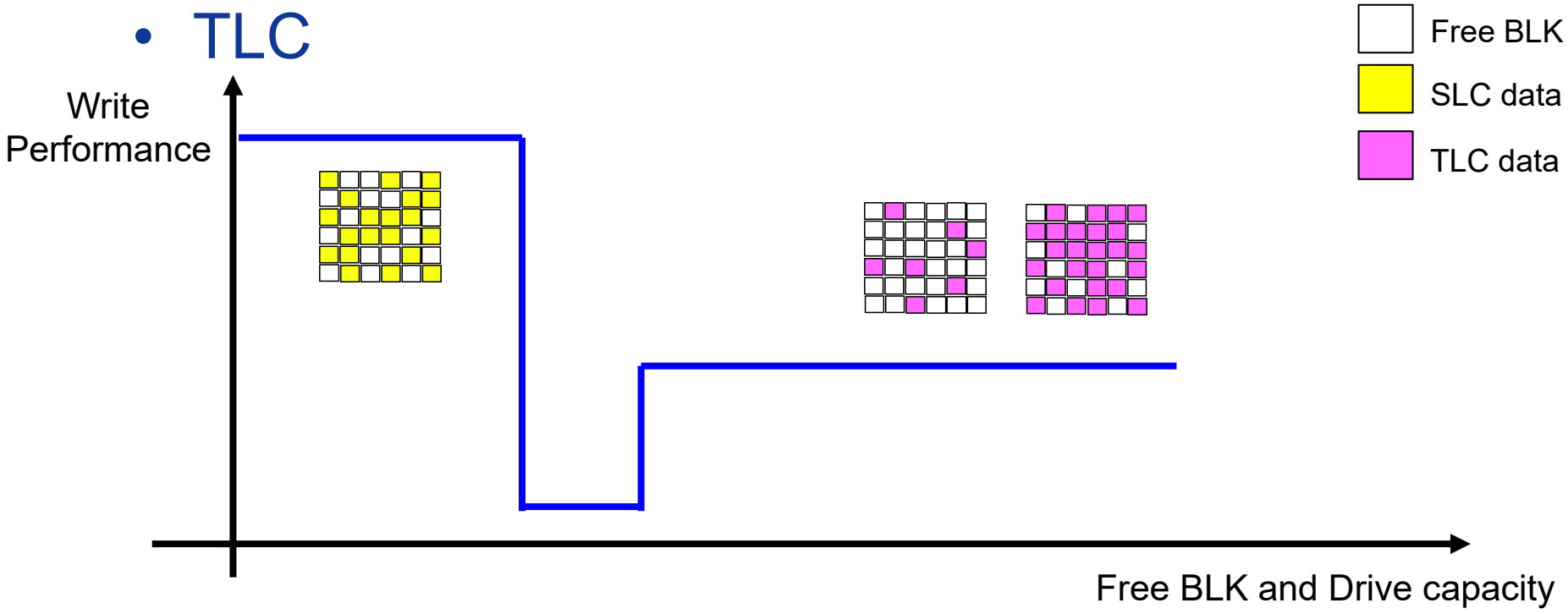
	3D-QLC	Phsion algo.
Cell architecture		
Multi-level per cell		
Error behavior (C2CI+Vth window)	Bad	1. C2CI-HB decode 2. C2CI-SB decode 3. Open BLK RAID 4. Dynamic program mode selection
Program algorithm	Multi-pass	
Performance	Bad	
Reliability (DR/RD…)	Bad	
DPPM issue	WL leakage (Program operation)	

Problems for Using QLC NAND

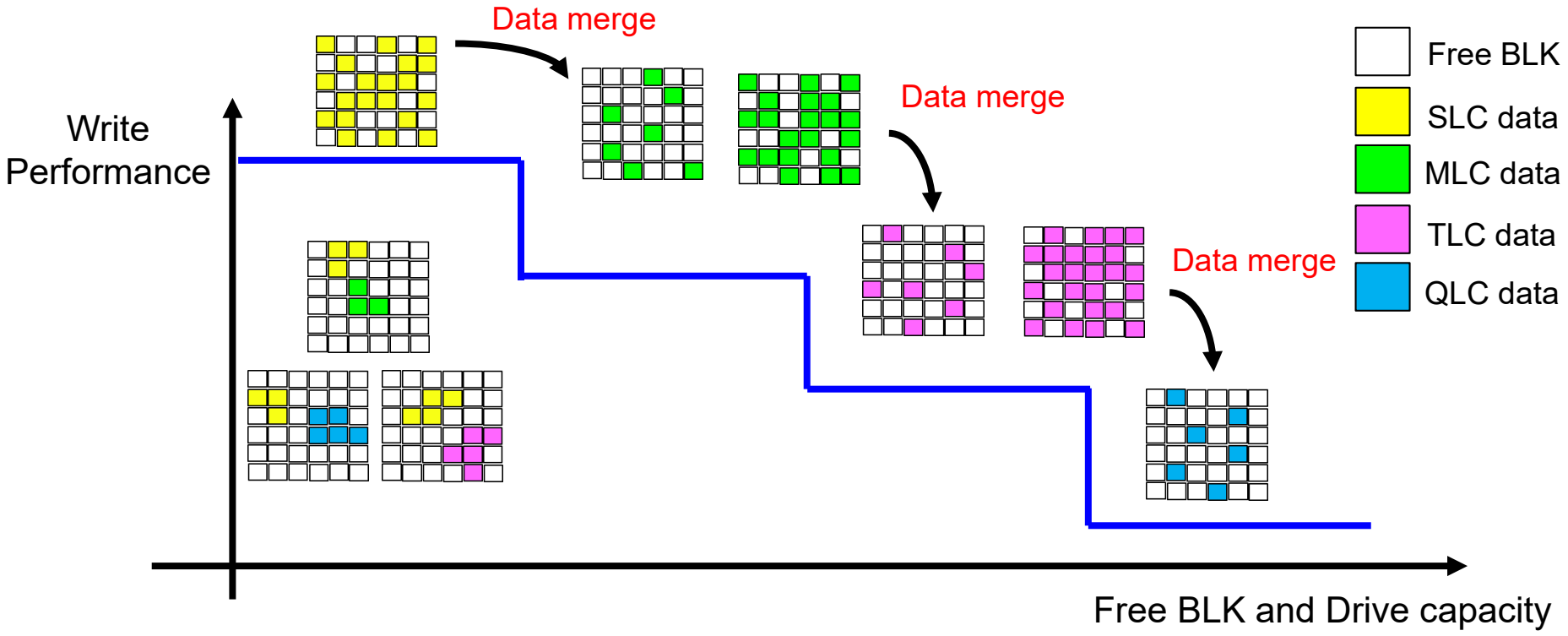
- Performance
- Reliability
  - DPPM
  - Tight Read Margin

Dynamic Buffer for TLC

- TLC



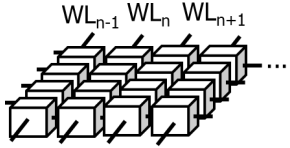
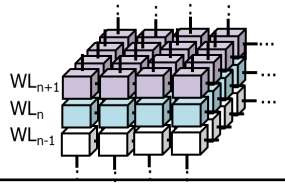
Dynamic Program Mode Selection



Problems for Using QLC NAND

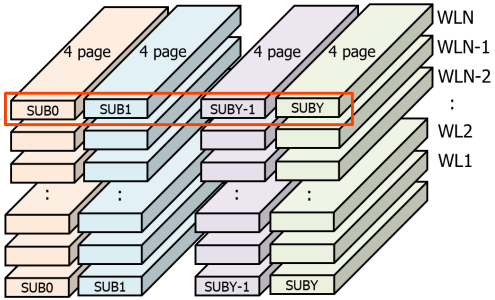
- Performance
- Reliability
  - DPPM
  - Tight Read Margin

DPPM Issue in 3D NAND Flash

	2D-TLC	3D-TLC	3D-QLC
Cell architecture			
DPPM issue	n/a	WL open/ short, WL leakage (Program operation)	

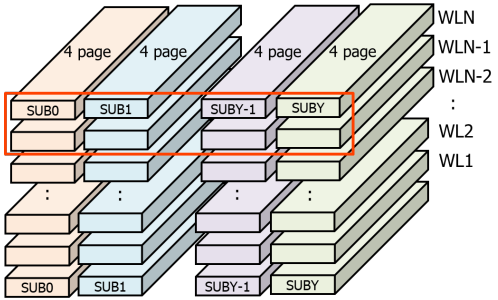
DPPM Issue in 3D NAND Flash

Case1: WL open



1-WL RAID Protection
SUB number= Y
RAM Buffer= 4*16*Y KB

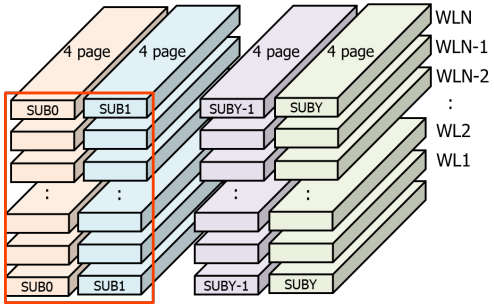
Case2: WL short



m-WL RAID Protection
SUB number= Y
RAM Buffer= 4*16*Y*m KB

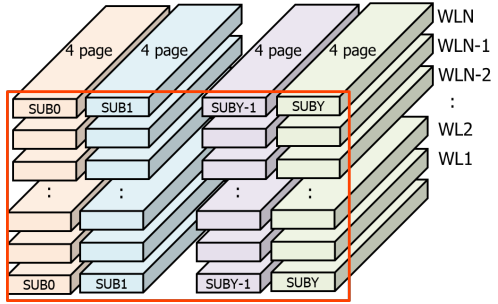
DPPM Issue in 3D NAND Flash

Case3: Memory hole open



SUB RAID is required
RAM Buffer= BLK size/ X
(X: number of SUB fail)

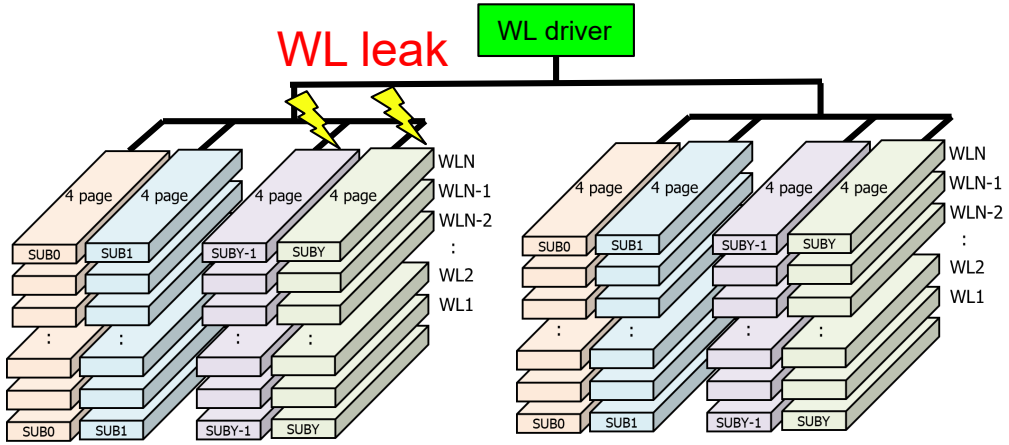
Case4: DSG WL induce BLK fail



BLK RAID is required
RAM Buffer= BLK size

DPPM Issue in 3D NAND Flash

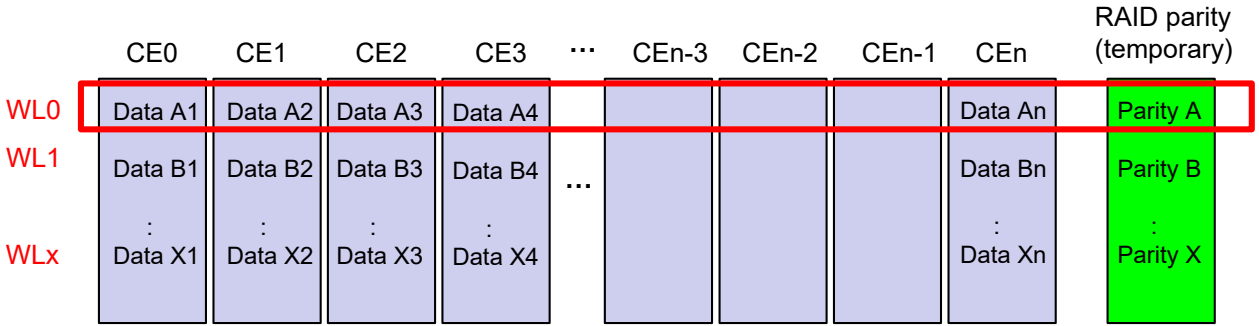
Case5: Multi-plane fail induces by WL leakage



Worse Case:
BLK RAID is required
RAM Buffer= BLK size * plane number
(3D NAND QLC BLK size~ 24~80MB)

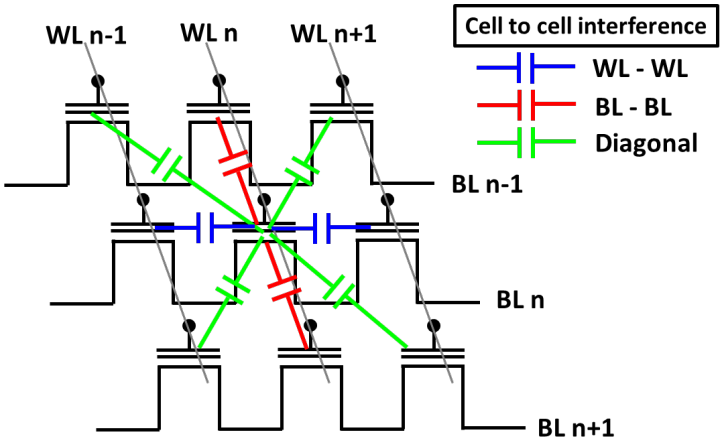
Open BLK RAID Protection

Host data Write: Open BLK

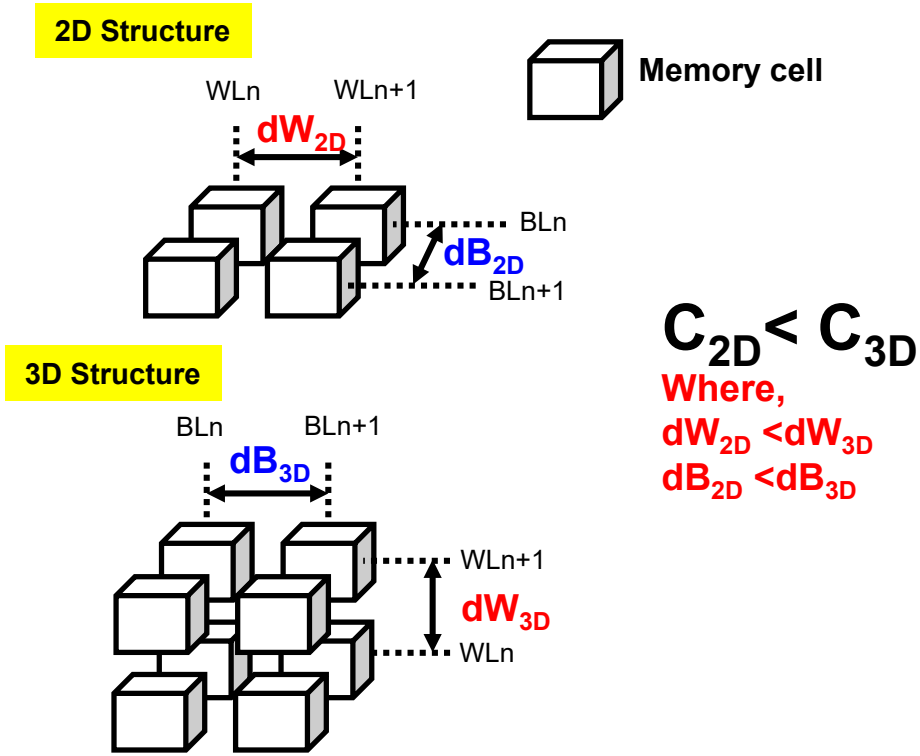


NOTE:
In order to protect Multi-WL and BLK fail case
Open BLK RAID can protect the data corruption
during program operation

What is Cell to Cell Interference (C2CI)



Capacitance~ 1/distance



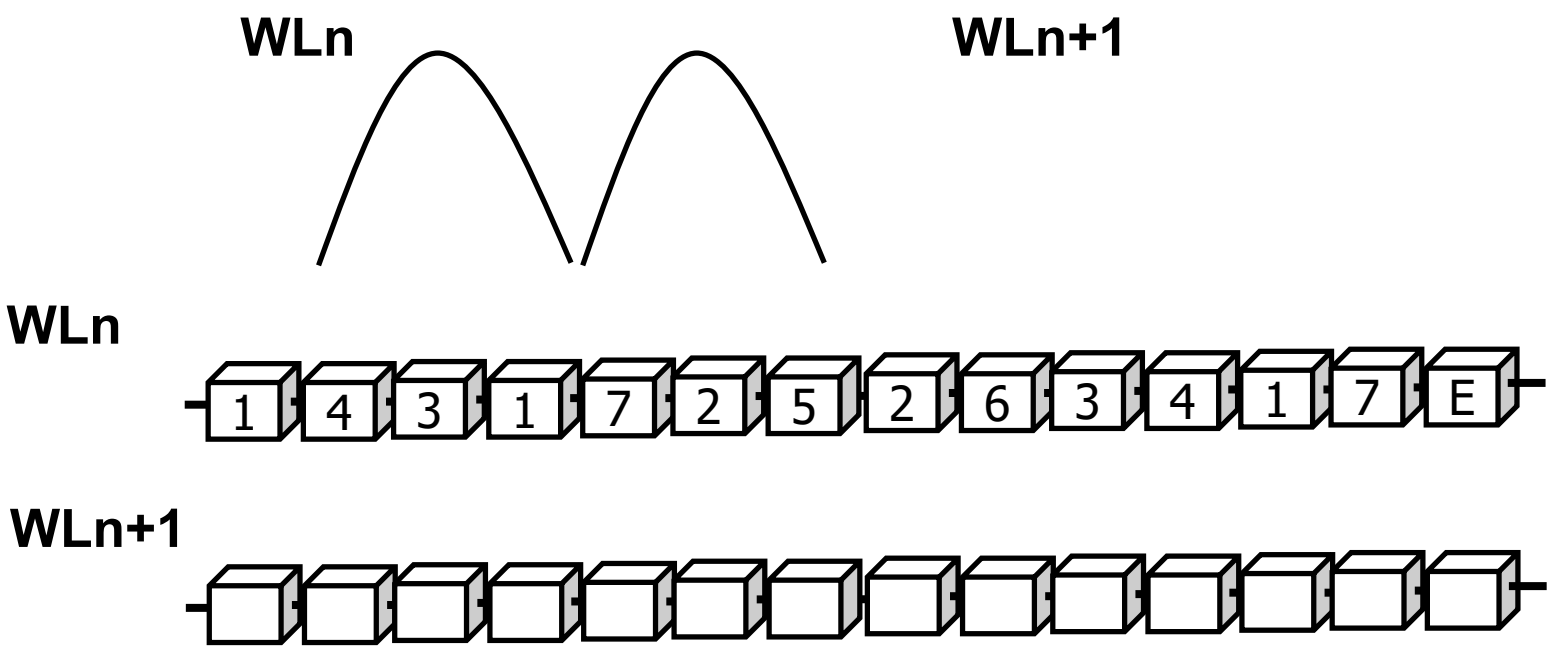
$C_{2D} < C_{3D}$

Where,

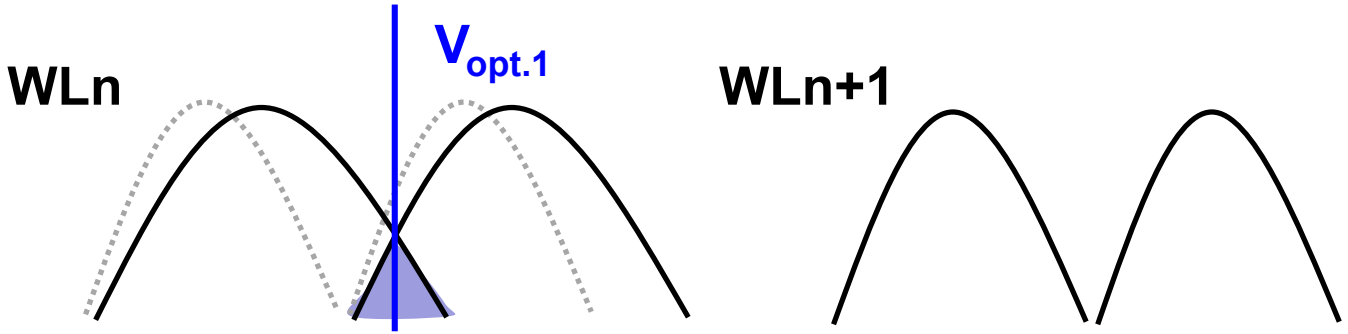
$dW_{2D} < dW_{3D}$

$dB_{2D} < dB_{3D}$

Cell to Cell Interference (C2CI)



Cell to Cell Interference (C2CI)



WLn

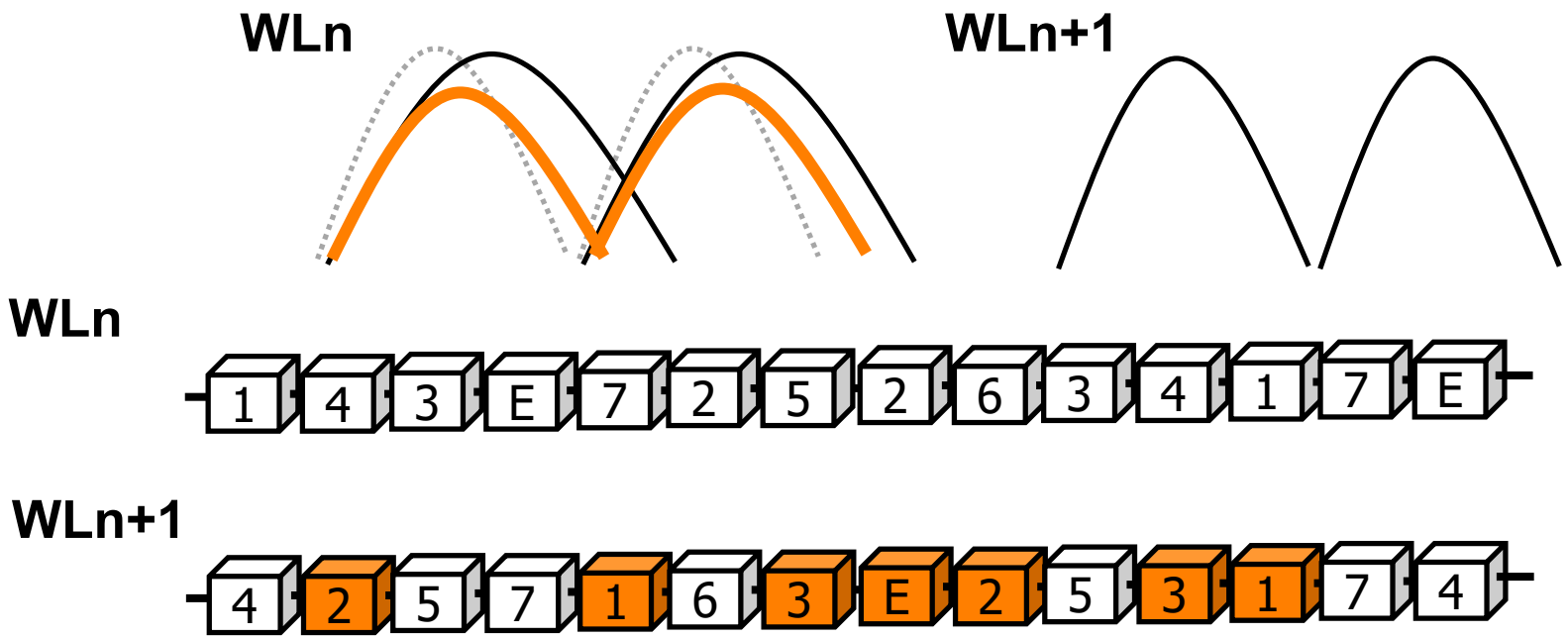
1	4	3	1	7	2	5	2	6	3	4	1	7	E

WLn+1

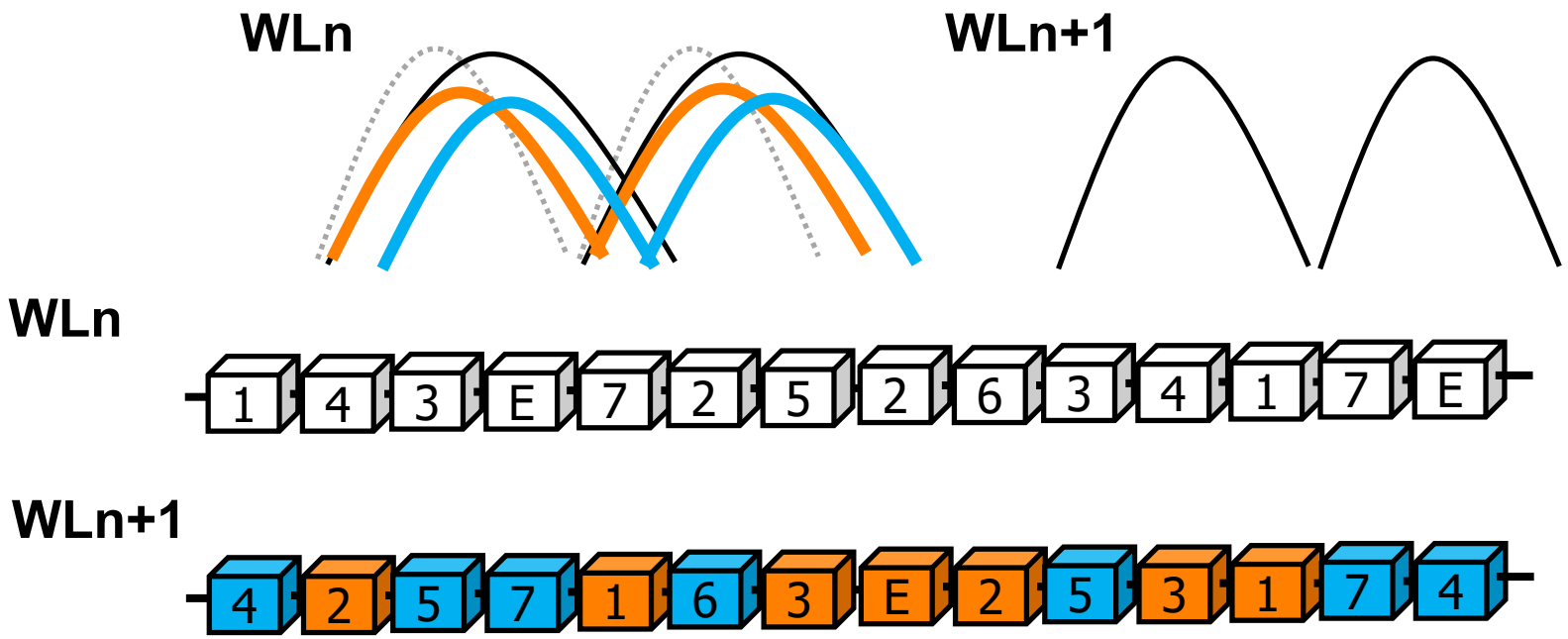
4	2	5	7	1	6	3	E	2	5	3	1	7	4

$$\Delta V_t(t) = V_{CG} + (C_\alpha / C_{FC}) V_\alpha - \beta t_{ox} / \gamma \ln\{(\beta A \cdot t / C_T t_{ox})$$

Cell to Cell Interference (C2CI)



Cell to Cell Interference (C2CI)



C2CI + Vth window

2D-TLC	3D-TLC	3D-QLC

w/o C2CI
(Program WLn only)

w/i C2CI
(Program WLn & WLn+1)

Error behavior (C2CI+Vth window)	Poor	Better	Bad

Single/Multi-pass Program algorithm

	2D-TLC	3D-TLC	3D-QLC
Program algorithm	Multi-pass	Single-pass	Multi-pass
Scenario 1 (1-pass)	n/a	8	n/a
Scenario 2 (2-pass)	n/a	n/a	8-16 program
			16-16 program
Scenario 3 (3-pass)	2-4-8 program	n/a	2-4-8 program
	8-8-8 program		
Performance	Poor	Better	Bad

NOTE: 2-4-8 program algorithm @ WLn
3 time program event is required (i.e. 3-pass)

- 1st program: input 1 page data (L page)
- 2nd program: input 2 page data (L+ M page)
- 3rd program: input 3 page data (L+ M + U page)

Performance Comparison

	2D-TLC	3D-TLC	3D-QLC
Performance	Poor	Better	Bad
Plane per die	2	Up to 4	Up to 4
Erase time (typ.)	5 ms/BLK	10 ms/BLK	10 ms/BLK
Program throughput (typ.)	15MB/s	80MB/s	20MB/s
Read throughput (typ.)	400MB/s	800MB/s	500MB/s

NOTE:
2D-TLC & 3D-QLC multi-pass program
System support is required

1. SLC to TLC/QLC copy-back method
   → High SLC endurance is required…
2. Pre-read with ECC correction method
   → System error handling is complex…
   (power cycle, open BLK, Fake 0xFF data…)

Reliability (DR/RD/XT…)

	2D-TLC	3D-TLC	3D-QLC
Reliability (DR/RD…)	Poor	Better	Bad
1yr Data retention	PE 300	PE 1500~3000	PE 1000
Read disturbed (BLRD)	3k	10k	<3k
Cross temperature	ΔT< 40°C	ΔT> 70°C	ΔT< 40°C

NOTE:
The major reliability concern is endurance cycle
System can cover others reliability item
(Ex. read disturbed can be detect and refresh)

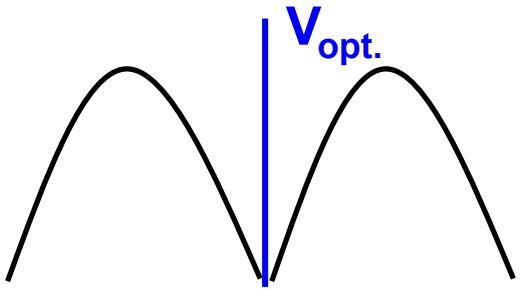
C2CI Cancelation

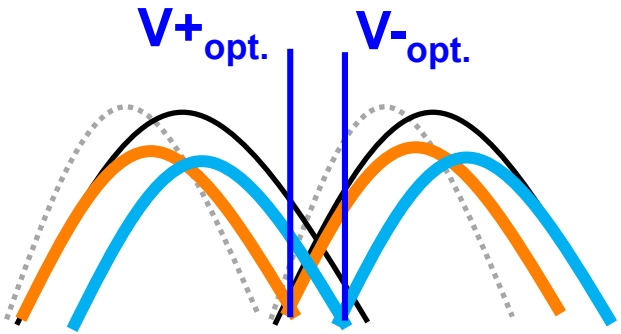
w/i C2CI

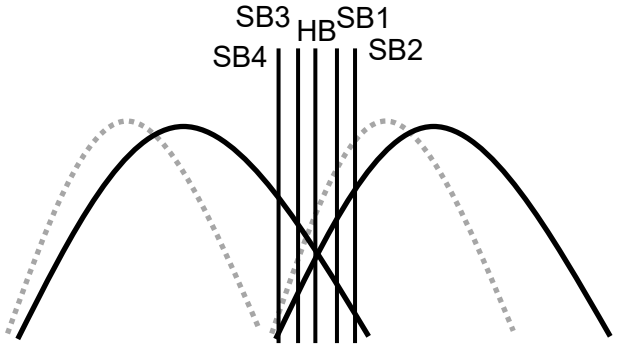
w/o C2CI

LDPC- HB decode

LDPC- SB decode







Default read (Opt.)

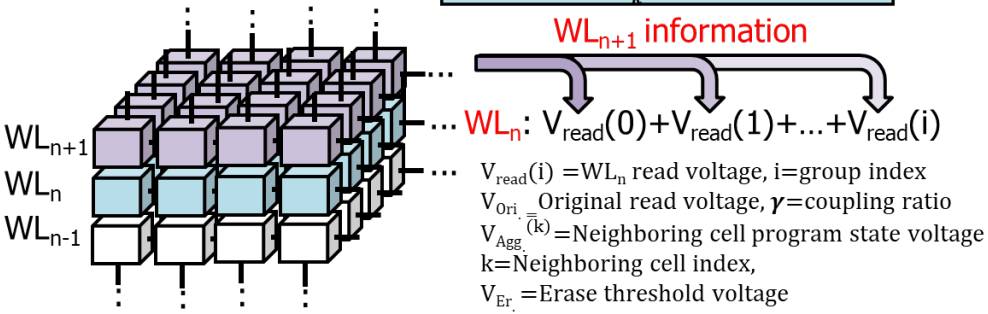
Read level 1 (Group^{+})
Read level 2 (Group^{-})

LLR set 1 (Group^{+})
LLR set 2 (Group^{-})

C2CI Cancelation- LDPC HB decode

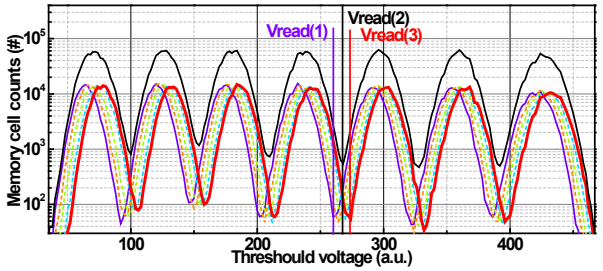
C2CI compensation algorithm- HB decode

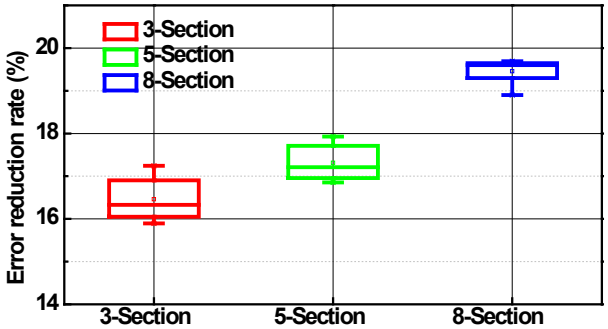
$$V_{read}(i) = V_{Ori.} + \sum_{k} ((V_{Agg.}^{(k)} - VEr_{.}) \cdot \gamma^{(k)})$$



$V_{read}(i)$ =WL_n read voltage, i=group index
$V_{Ori.}$ =Original read voltage, γ=coupling ratio
$V_{Agg.}^{(k)}$ =Neighboring cell program state voltage
k=Neighboring cell index,
$V_{Er.}$ =Erase threshold voltage

Correction capability improvement

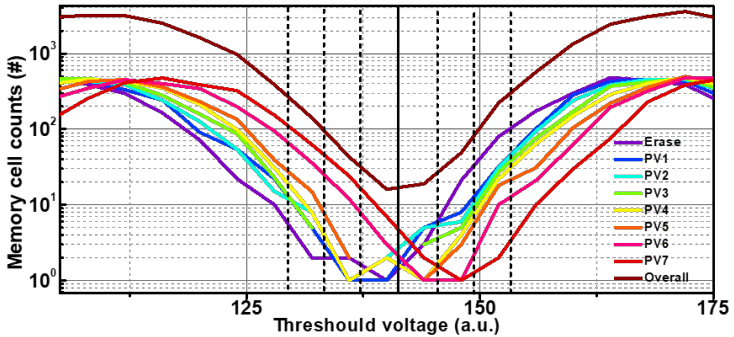




C2CI Cancelation- LDPC SB decode

C2CI compensation algorithm- SB decode

$$RI(j) = Log\left[\frac{Exp\left\{-\frac{1}{2\sigma_{n+1}^2}\left(V_{SB}^{(j,n+1)}\right)^2\right\} - Exp\left\{-\frac{1}{2\sigma_{n+1}^2}\left(V_{SB}^{(j,n+1)} - V_{read}(i)\right)^2\right\}}{Exp\left\{-\frac{1}{2\sigma_n^2}\left(V_{SB}^{(j,n)}\right)^2\right\} - Exp\left\{-\frac{1}{2\sigma_n^2}\left(V_{SB}^{(j,n)} - V_{read}(i)\right)^2\right\}}\right] \cdot \beta^{(j)}$$



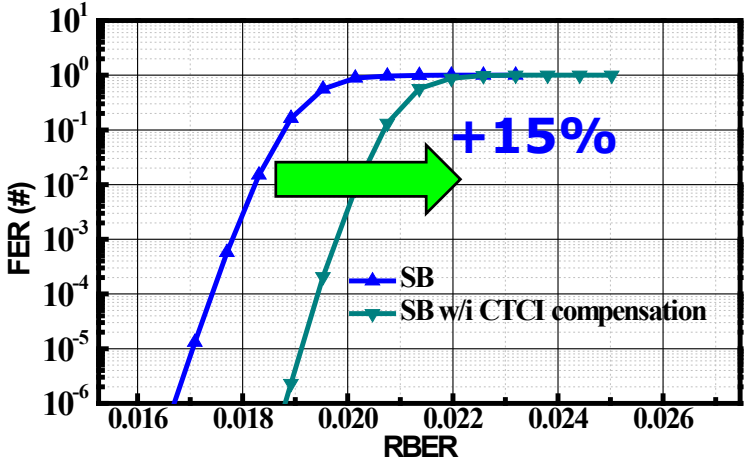
RI(j) =Reliability information- LLR

j=SB rank index, $V_{SB}^{(j,n)}$ =SB read voltage

n=Program state, σ_n= Standard deviation of program state n

$\beta^{(j)}$= Shrink coefficient for SB rank j

Correction capability improvement



Conclusion

- Dynamic program buffer is proposed to optimize the system performance.
- New block RAID algorithm is proposed to reduce the SRAM size and parity size for 3D NAND Flash
- Adaptive DSP is used to improve the correction capability by modifying the LLR value according data in adjacent WL.