Flash Memory Summit

FLASH at the Speed of FLASH
FLASH at the Cost of DISK

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Agenda

- Missing IOPS
- Efficient Storage
- DPU
- Storage evolution

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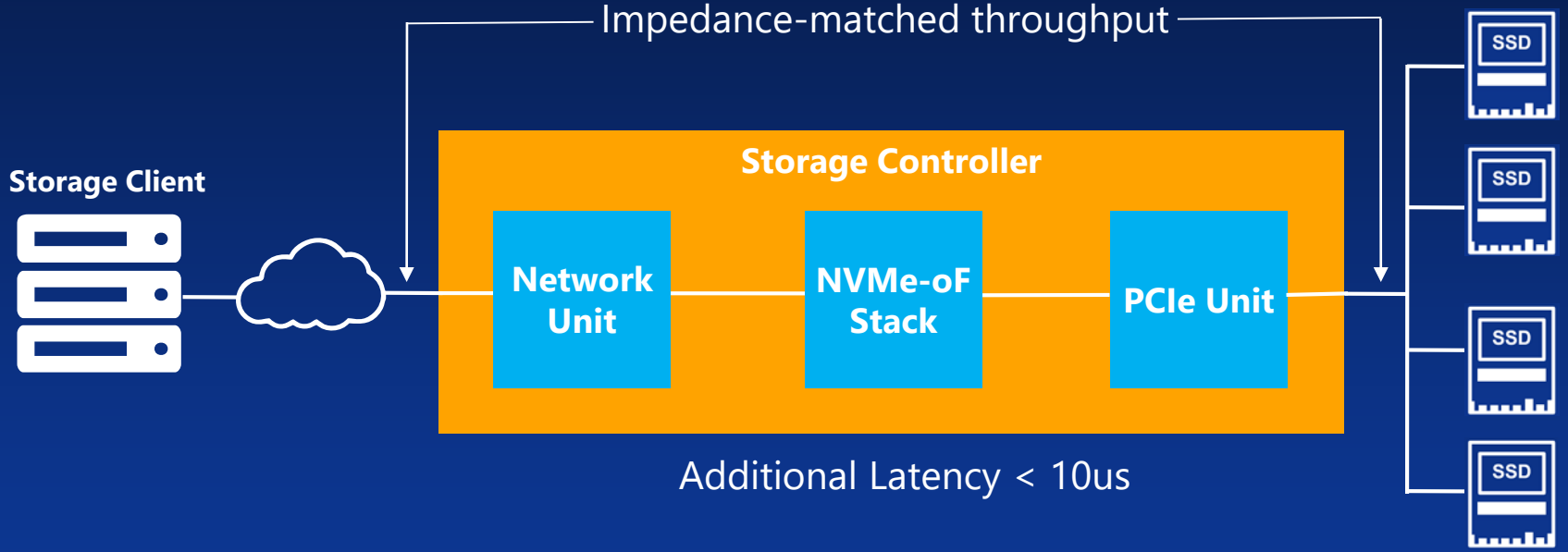
Disaggregated Storage Architecture

Flash Memory Summit

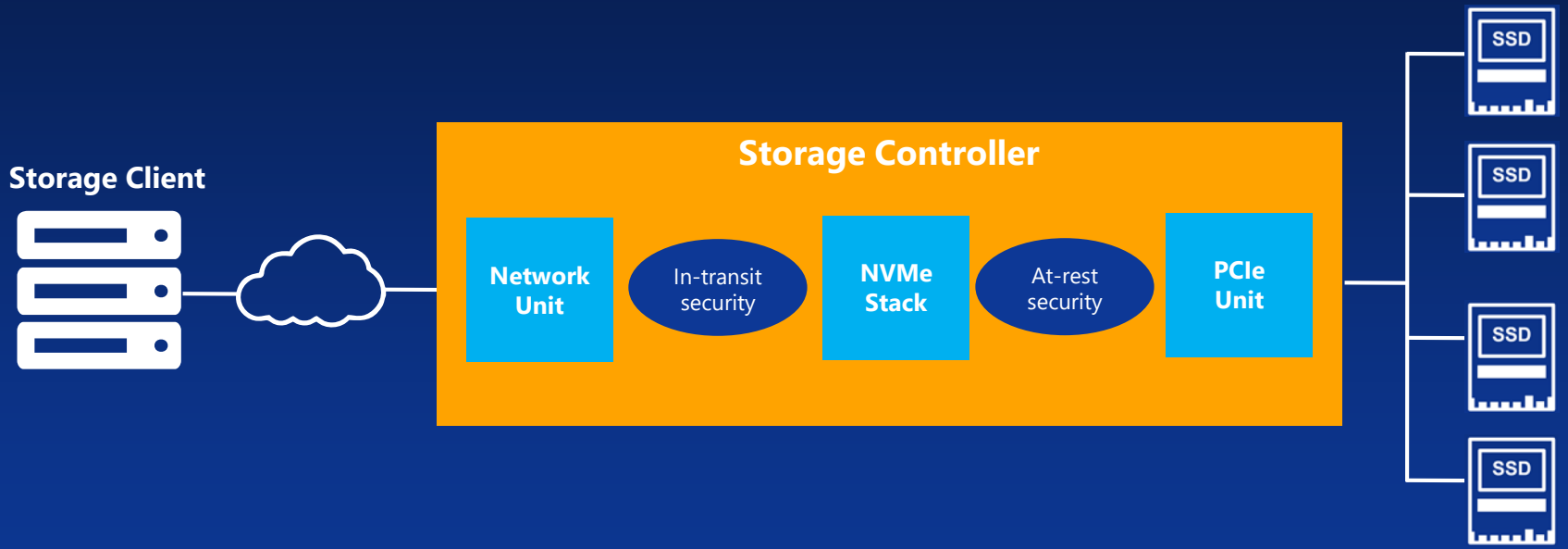
Looking for the Missing IOPS

High IOPS, Low Latency controller



Controller must enable line rate SSD IOPS to clients

+ In-line Security at No Impact to Performance and Cost



Provide Robust E-W Network Security and At-Rest Security

Agenda

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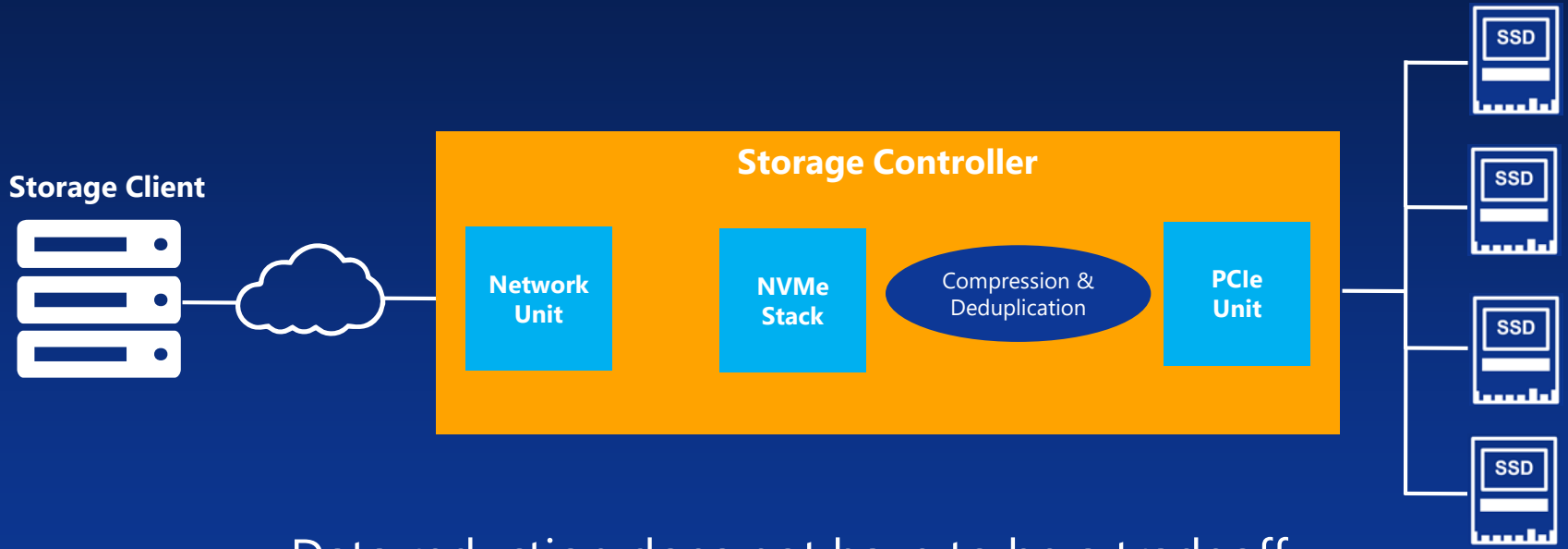
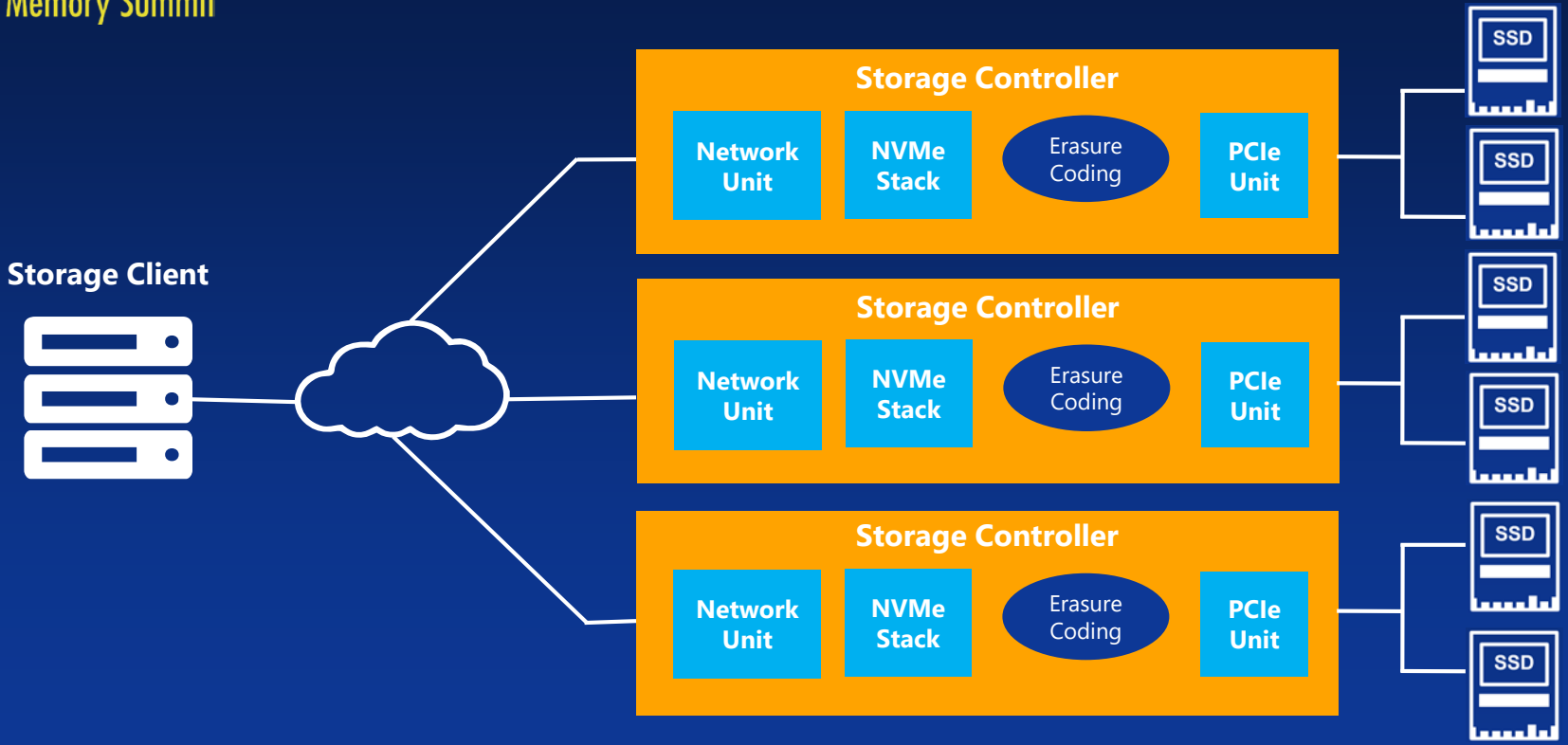
+ In-line Data Reduction at No Impact to Performance and Cost



Data reduction does not have to be a tradeoff between compression ratio and throughput

+ In-line Data protection at No Impact to Performance and Latency

+ Higher Reliability with Lower Storage Overhead



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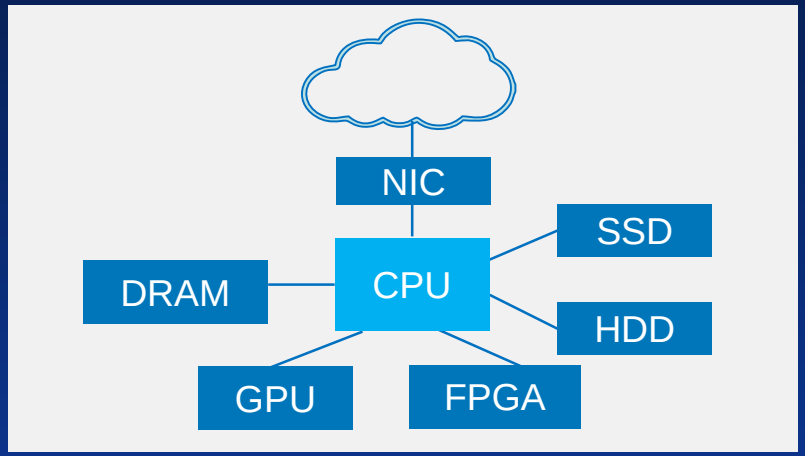
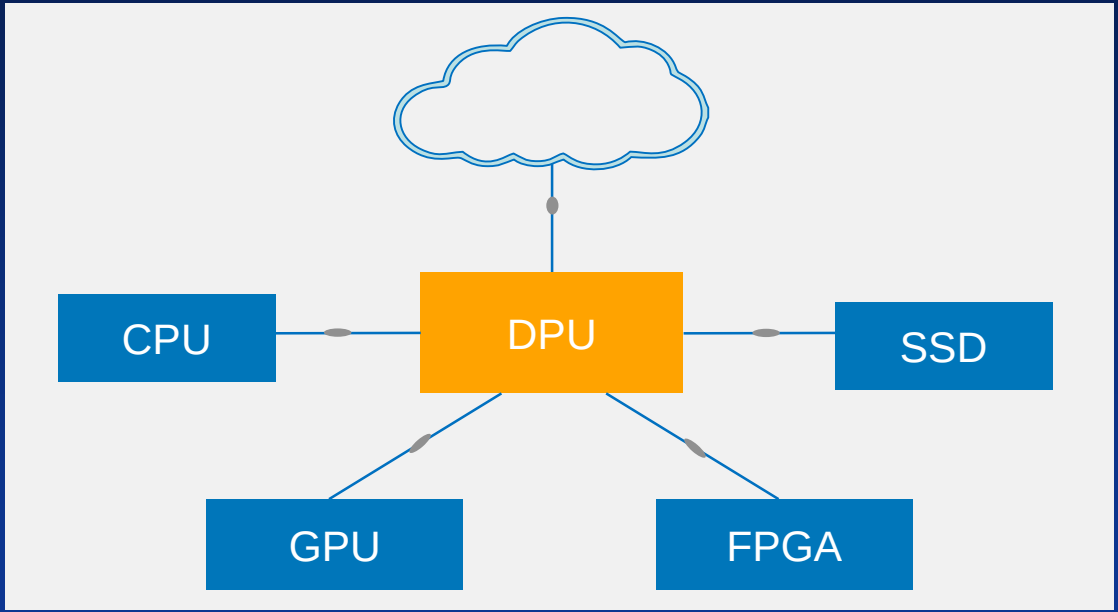
- Missing IOPS
- Efficient Storage
- DPU
- Computational Storage

Today - Data Centers are still based on Legacy PC-like Architecture



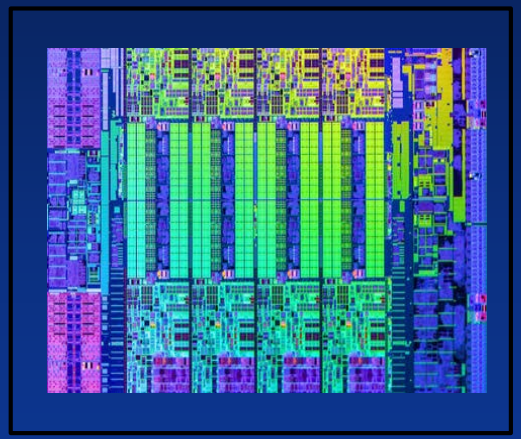
… with some added accelerators
But CPU remains the bottleneck

Introducing … The Fungible DPU
A new category of programmable microprocessor



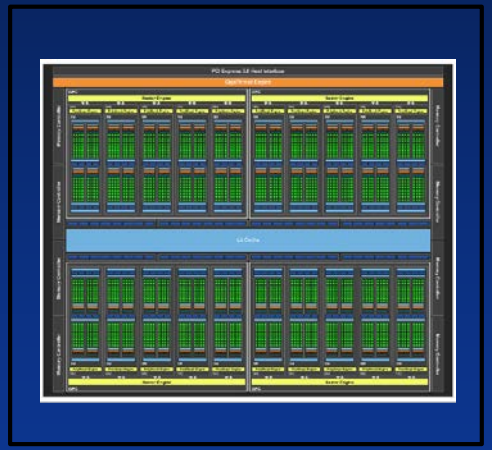
The Data Processing Unit (DPU)

CPU



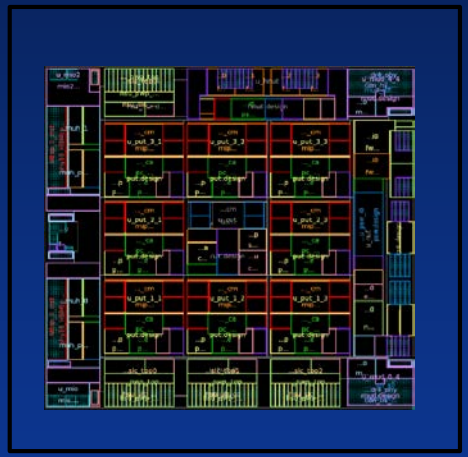
General-purpose application processing

GPU



Complex math, AL/ML workloads

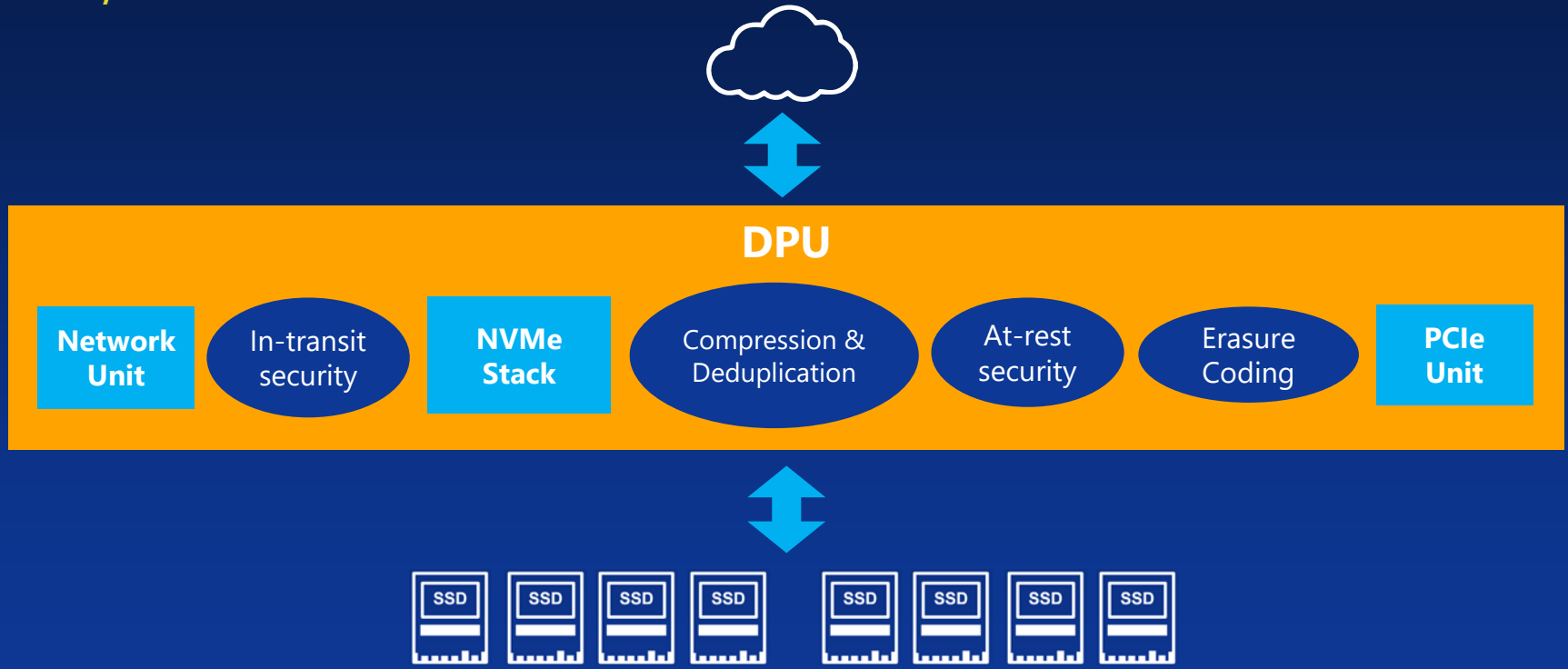
DPU



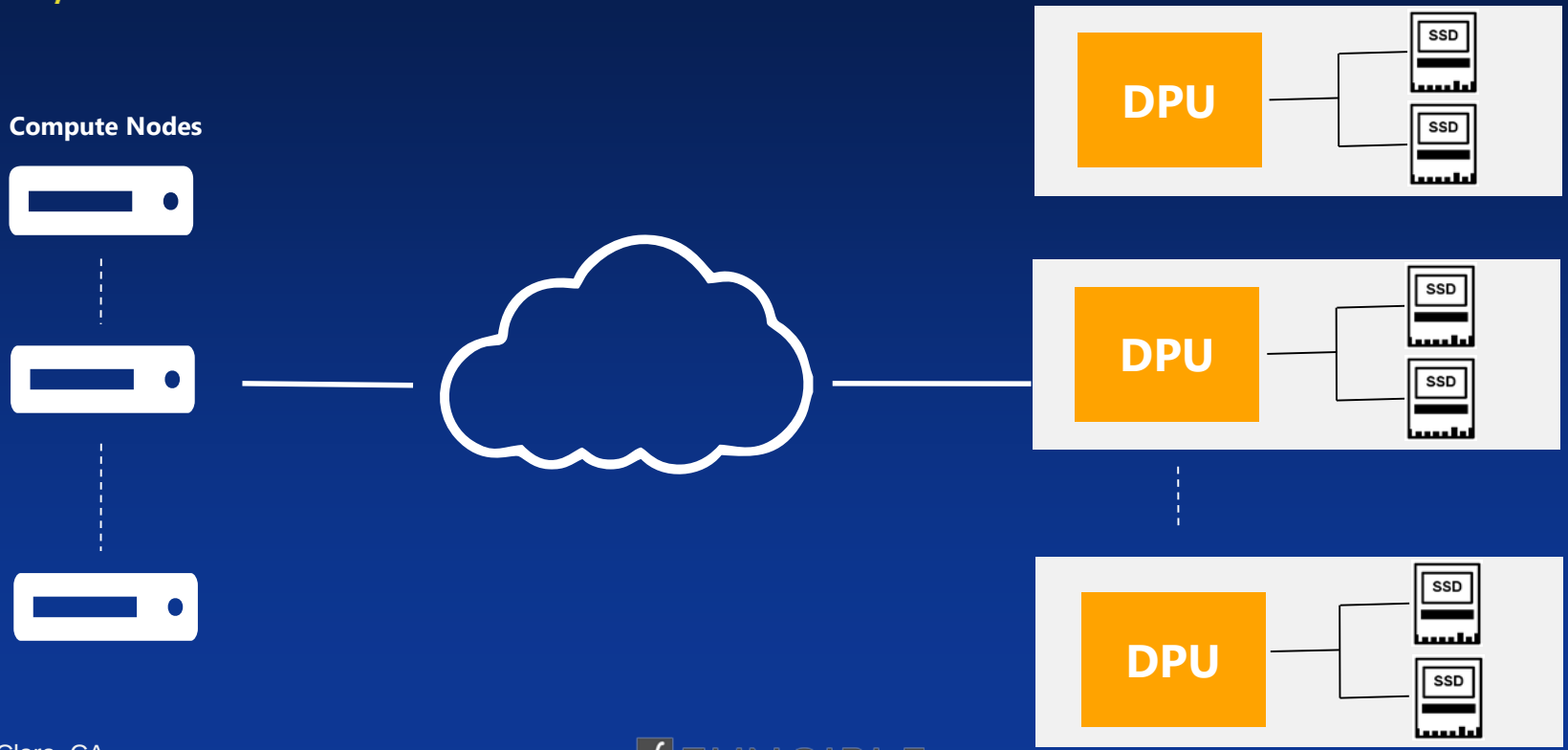
Data-centric infrastructure workloads

Secure Scale-Out Storage

@ the speed of FLASH & the $ of DISK



True Scale-Out Disaggregated Storage



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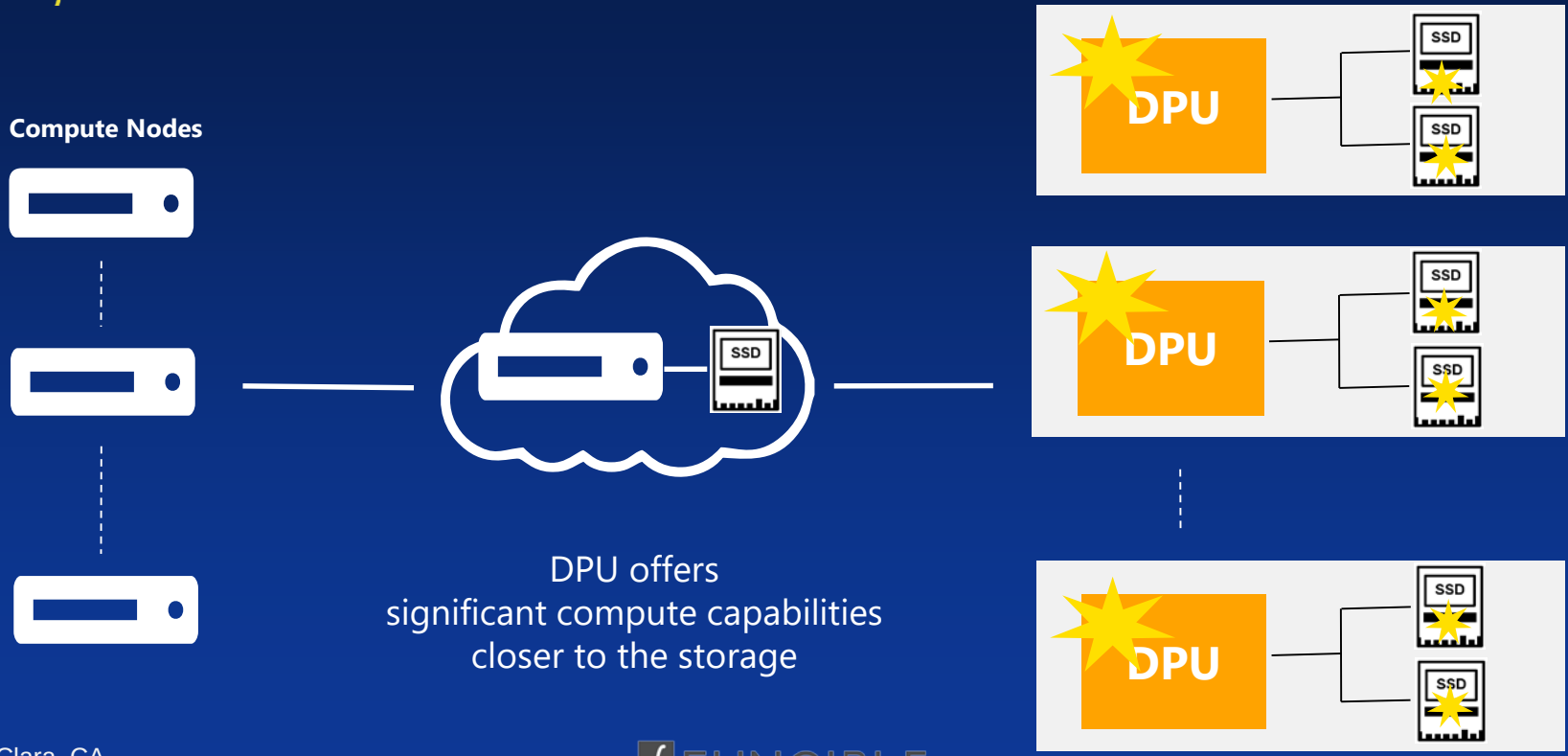
Storage Evolution



DPU offers
significant compute capabilities
closer to the storage

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We are hiring !