Component-Level Characterization of 3D TLC, QLC, and Low-Latency NAND

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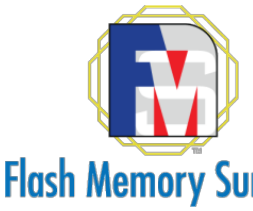
Agenda

- Importance of 3D NAND Characterization
- 3D TLC, QLC, and Low-Latency NAND
  - Characterization of 3D QLC
  - Characterization of 3D TLC
  - Characterization of Low-Latency NAND



Importance of 3D NAND Characterization

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- Component-level characterization of 3D NAND is essential for end-use applications
  - Characterization feeds into controller design – many avenues for optimization
  - Characterization that closely matches expected use-case is the most valuable
- 3D NAND presents characterization challenges – but also opportunities
  - IBM FlashSystem leverages extensive component-level characterization to produce leading-edge controller design

3D TLC, QLC, and Low Latency NAND

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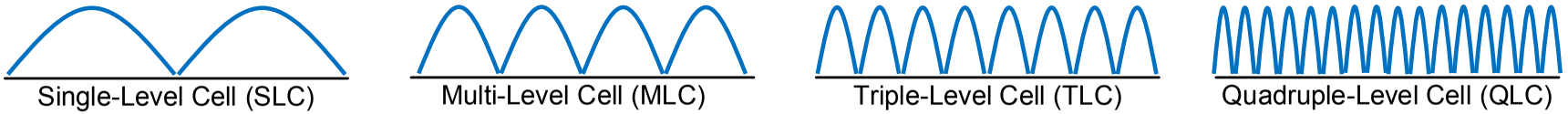
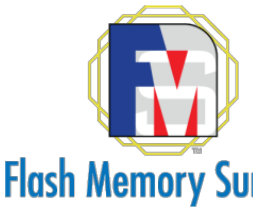
- 2D NAND limited to traditional SLC and MLC
  - Early attempts at 2D TLC had limited utility
- Transition to 3D NAND enabled **TLC** & **QLC**
  - Competition with emerging memory technologies precipitated **Low-Latency NAND** (3D SLC)
- All three 3D NAND technologies present certain characterization challenges





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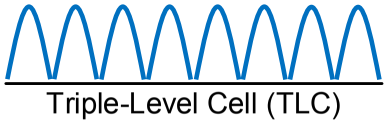
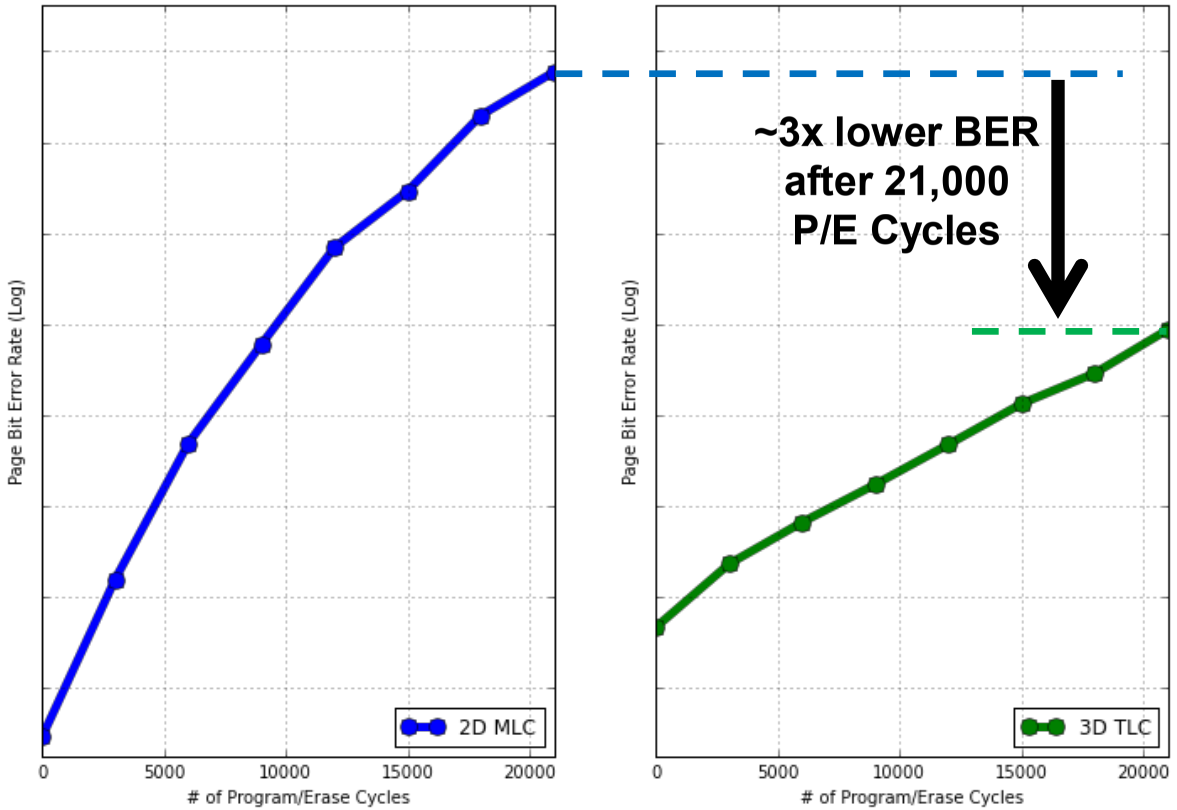
Characterization of 3D TLC

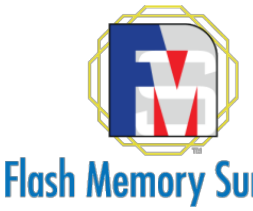
- Transition to 3D NAND enabled TLC for mainstream applications
  - Enterprise, consumer
- 3D TLC has rapidly displaced 2D MLC
- Characterization of TLC depends on expected use-case
  - The more aggressive the application, the more demanding the characterization



3D TLC Displays High Endurance

- 1st gen. 3D TLC showed superior cycling endurance over prior-gen. 2D MLC
  - High quality of 3D TLC enabled wide adoption
- While excellent for end-use case, transition to TLC presented challenges for characterization





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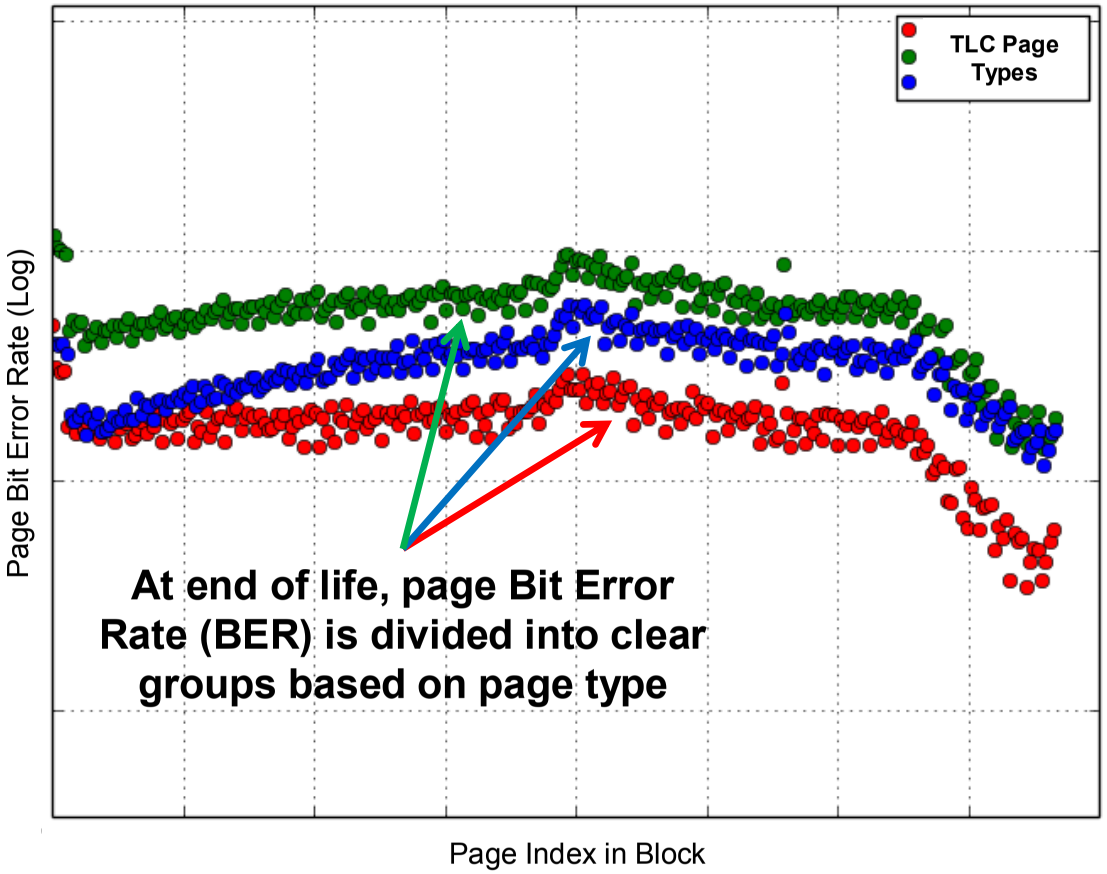
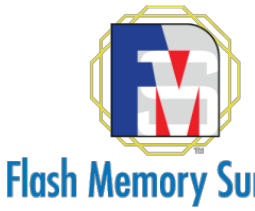
Proliferation of TLC Page Types

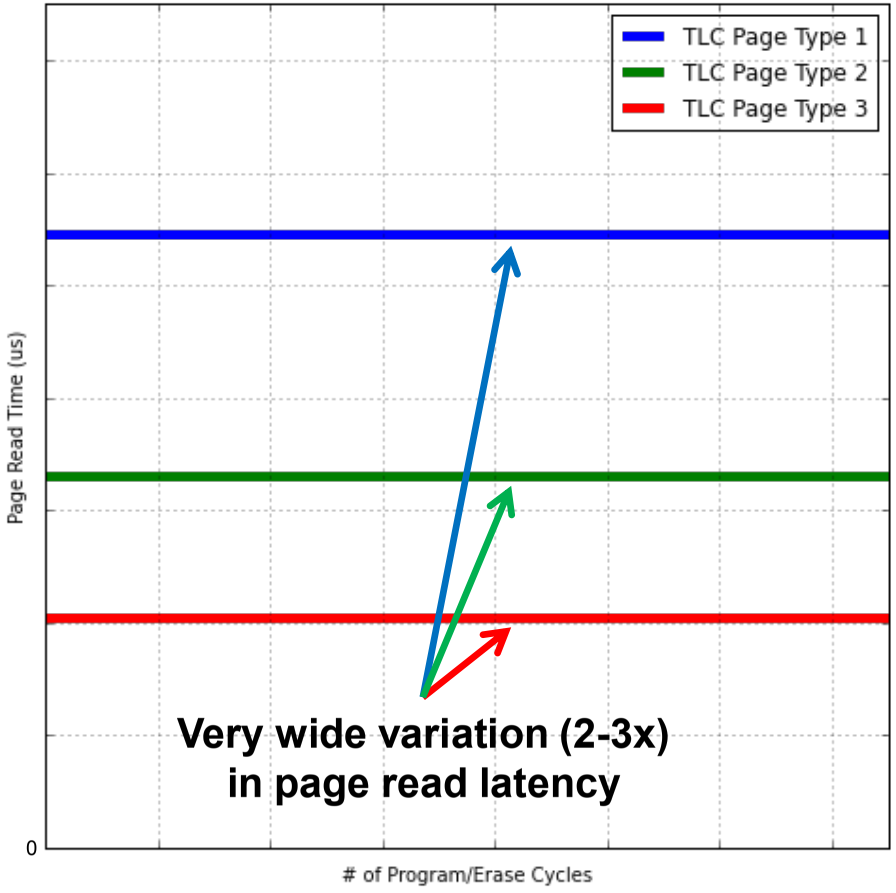
- TLC blocks have at least 3 different page types with different characteristics
  - Some manufacturers include MLC and SLC pages as well
- Full characterization requires understanding behavior of each page type
  - Worst-case page determines Bit Error Rate (BER) limits
  - Page quality can vary across block (3D cell stack)
  - Different page types respond differently to various NAND failure modes (retention, read disturb)





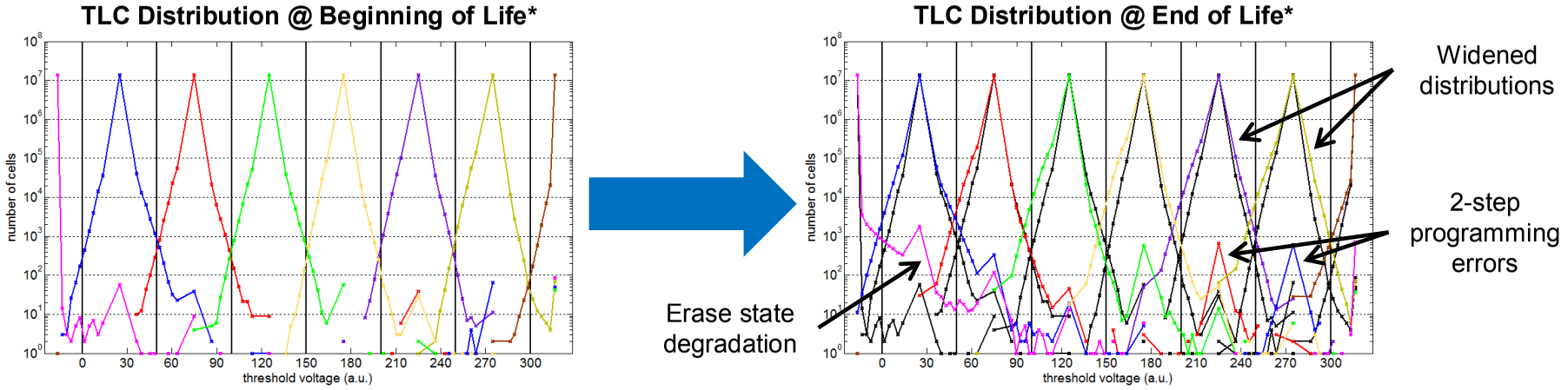
Variation of Read Latency by Page Type

- Different TLC page types often have different read latency
  - MLC and SLC pages, if present, have different latency as well
- Should characterization focus on worst-case read time or average read time? Depends on use-case
  - Controller design must be robust against varying read latency



TLC NAND Cells Increasingly Crowded

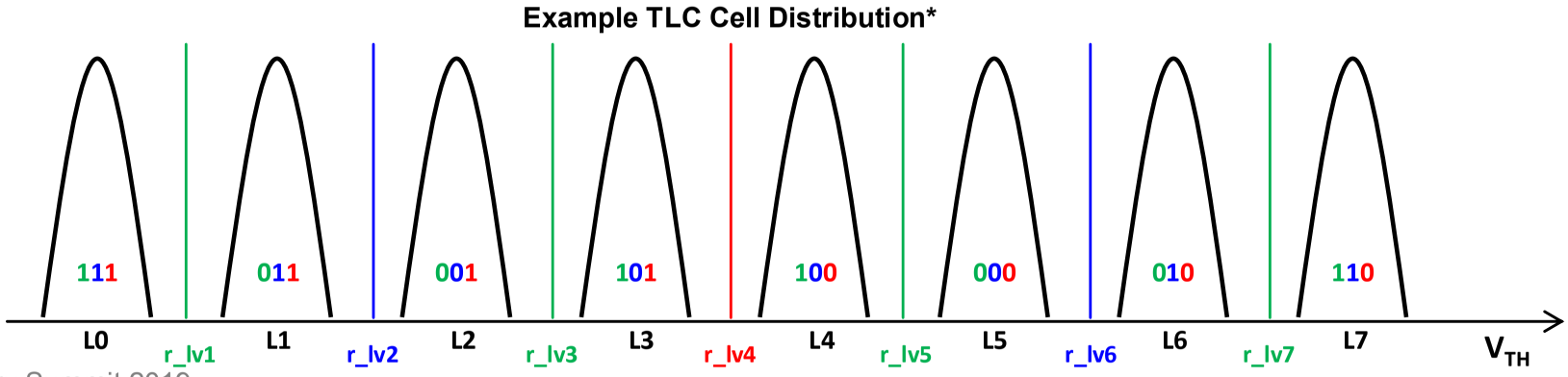
- TLC NAND cells must support 8 independent cell states
  - Cell distributions packed tightly – little margin for error
  - As cells are subjected to cycling stress, problems arise
  - Extensive characterization required to understand impacts



*For more information, see N. Papandreou *et al*., "Characterization and Analysis of Bit Errors in 3D TLC NAND Flash Memory," *2019 IEEE International Reliability Physics Symposium (IRPS)*, Monterey, CA, USA, 2019, pp. 1-6.

Read Voltage Threshold Management

- 8 independent cell states require 7 individual read thresholds to discriminate between
- How aggressive is your read voltage threshold management?
  - Reactive recovery only? Proactive application of manufacturer read shift tools? Active tracking of all optimal read thresholds?
    - Trade-off between capability and complexity – characterization required to validate approach



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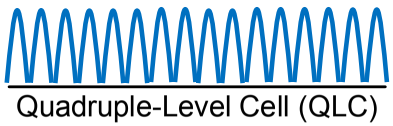
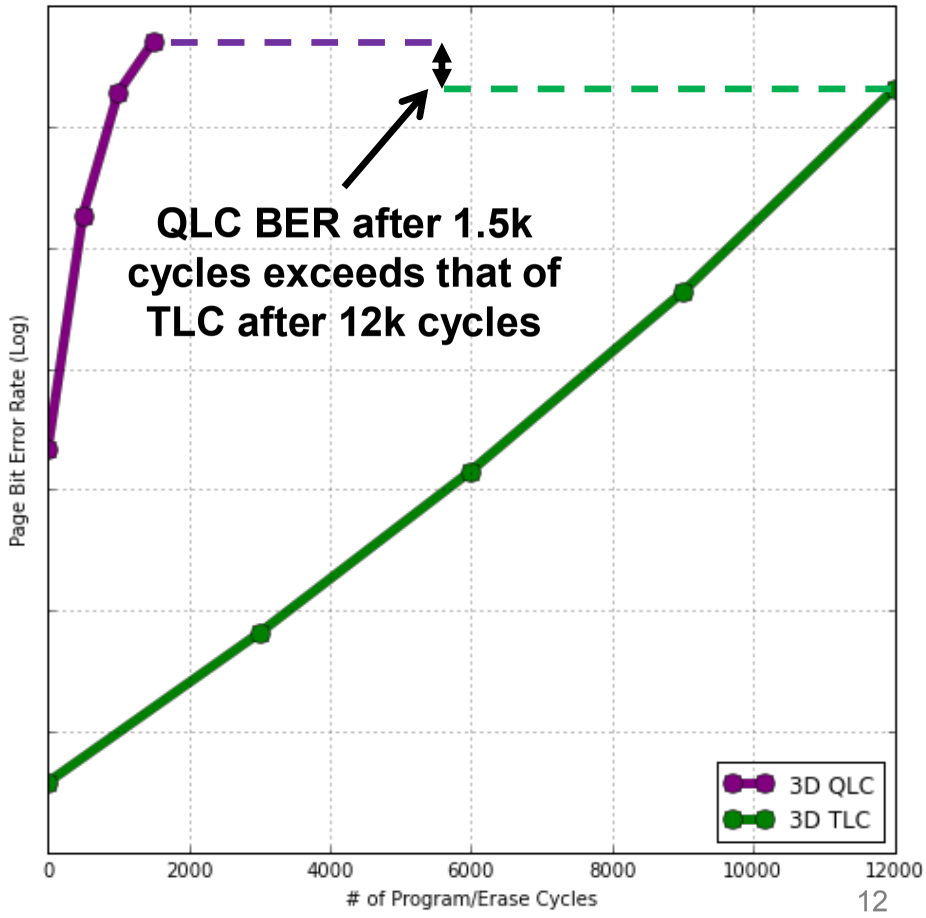
Characterization of 3D QLC

- Transition to 3D NAND has also enabled development of QLC NAND
  - Improved density and $/GB at cost of reduced endurance and timing parameters
  - Initial focus on read-intensive applications
- 3D QLC characterization has all the challenges of 3D TLC, only more so
  - Plus, some new complications



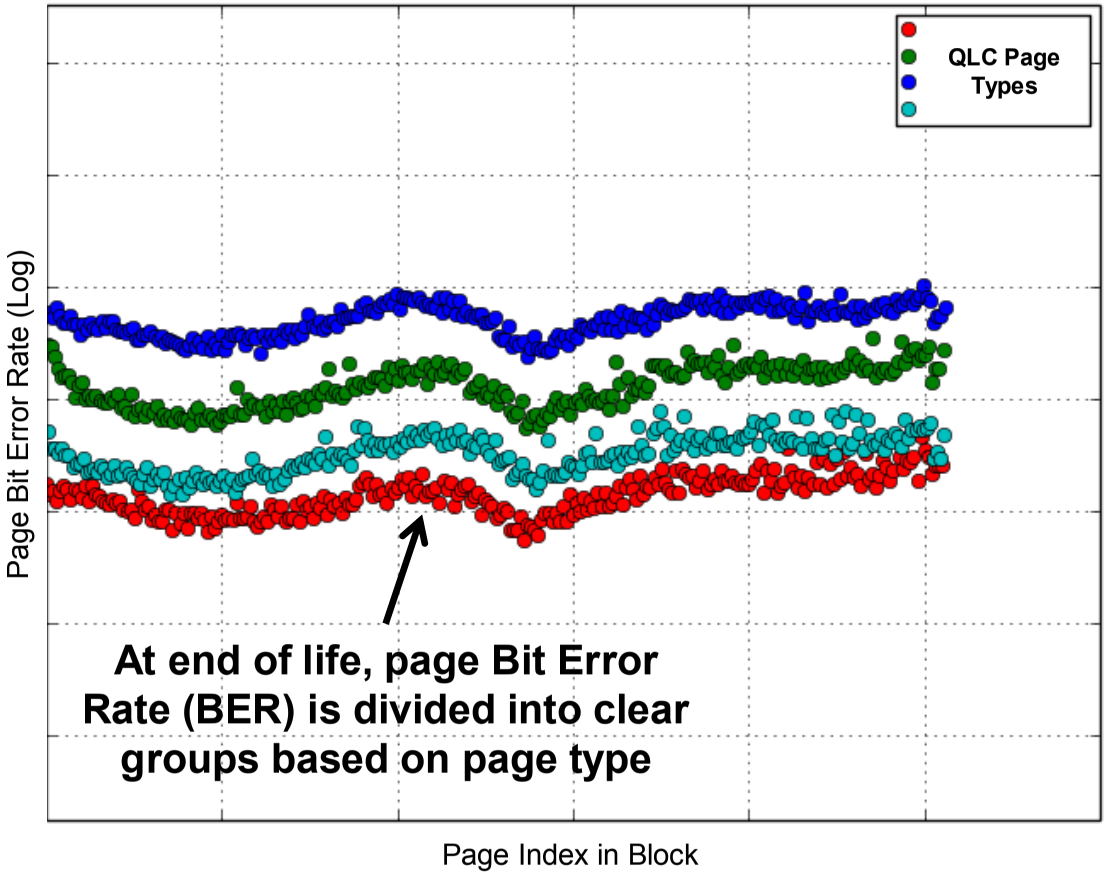
3D QLC Shows Drastically Reduced Endurance

- 3D QLC shows significantly reduced endurance relative to TLC
  - Cycling endurance less important for read-intensive applications
- Limited endurance of QLC places restrictions on end-use, but actually makes characterization faster!



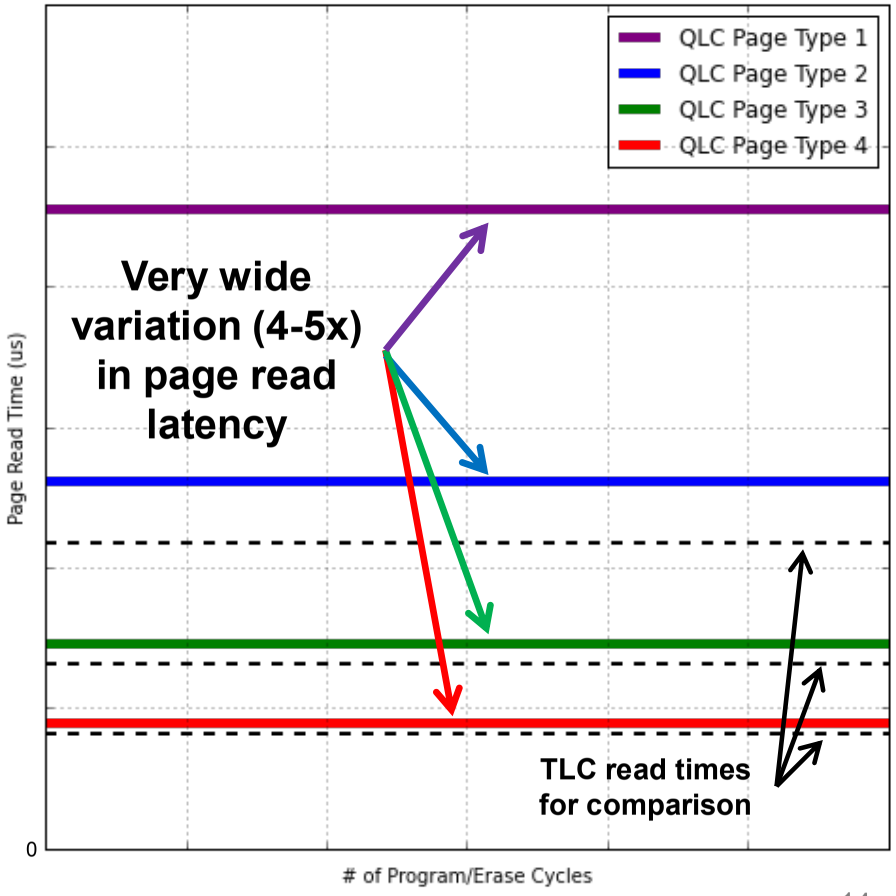
3D QLC: Even More Page Types

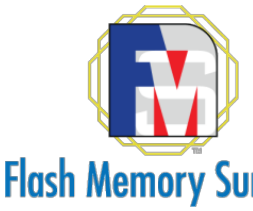
- QLC blocks have at least 4 different page types
  - Some manufacturers include TLC and SLC pages as well
- Understanding behavior of each page type is particularly important for QLC – there is little margin for error, and every little bit helps



3D QLC: Even More Read Latency Variation

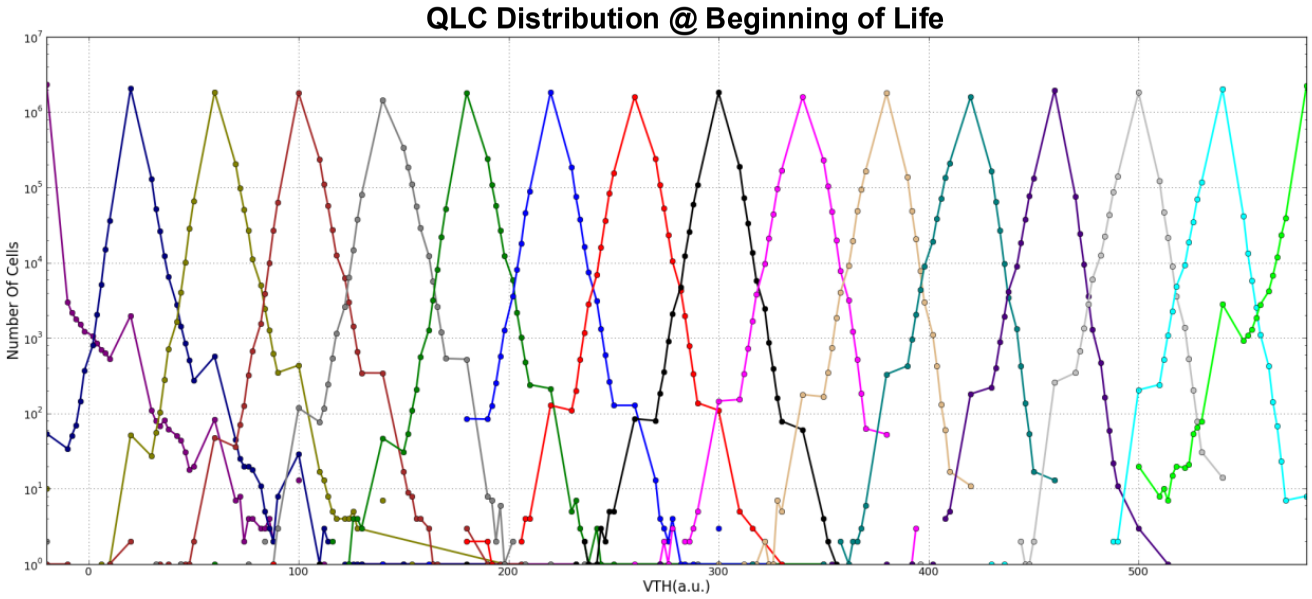
- Average read latency for QLC is elevated over that of TLC
  - Read latency is important design consideration for read-intensive applications
- Wide variation in QLC page-type read latency
  - Read latency variation is even more pronounced than in TLC
  - Controller design must be robust against read latency uncertainty





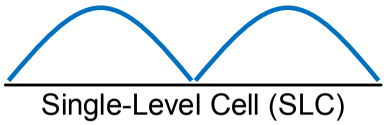
3D QLC: Even More Crowded Cells

- QLC has 16 states and 15 read thresholds
  - Very little margin for error, especially after cycling wear
  - Management of read voltage thresholds more complex than in TLC
    - Any approach requires extensive characterization and validation



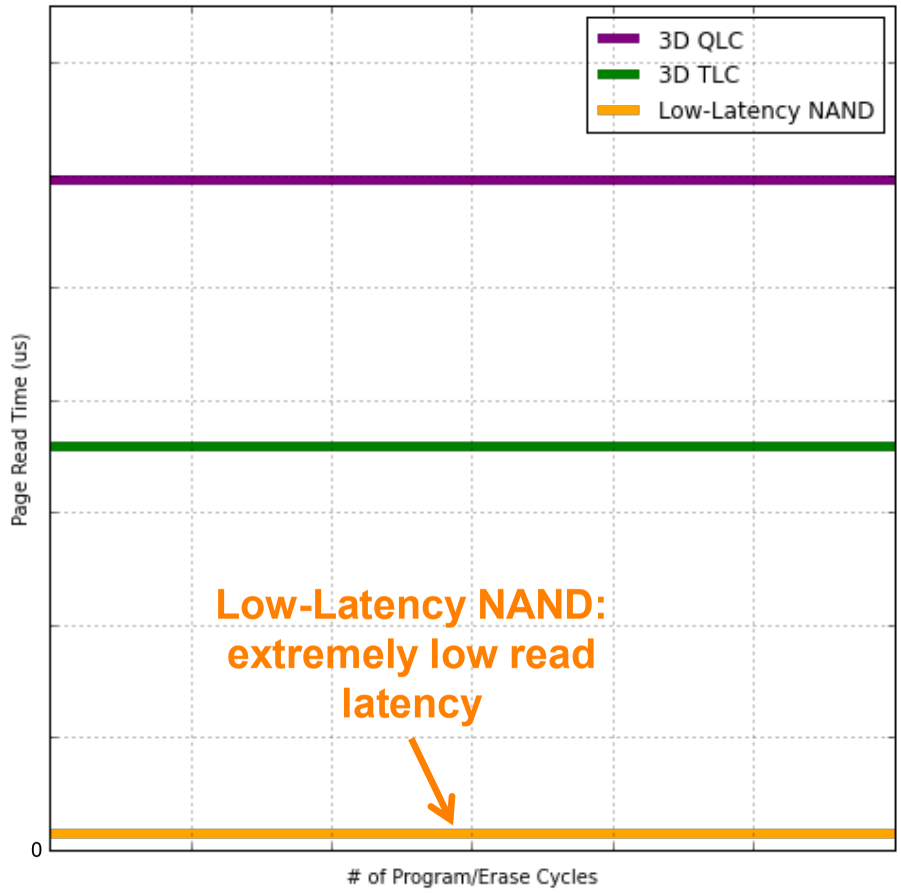
Characterization of Low-Latency NAND

- Low-Latency NAND being developed by some manufacturers to challenge emerging memory
  - Designed to fit niche between traditional NAND and DRAM
- Low-Latency NAND is 3D SLC optimized for very low read latency (single-digit microseconds)
  - 3D TLC NAND read latency is ~75us, DRAM is ~50ns
  - Trade-off: reduced capacity and increased $/GB
- Low-Latency NAND comes with its own characterization challenges



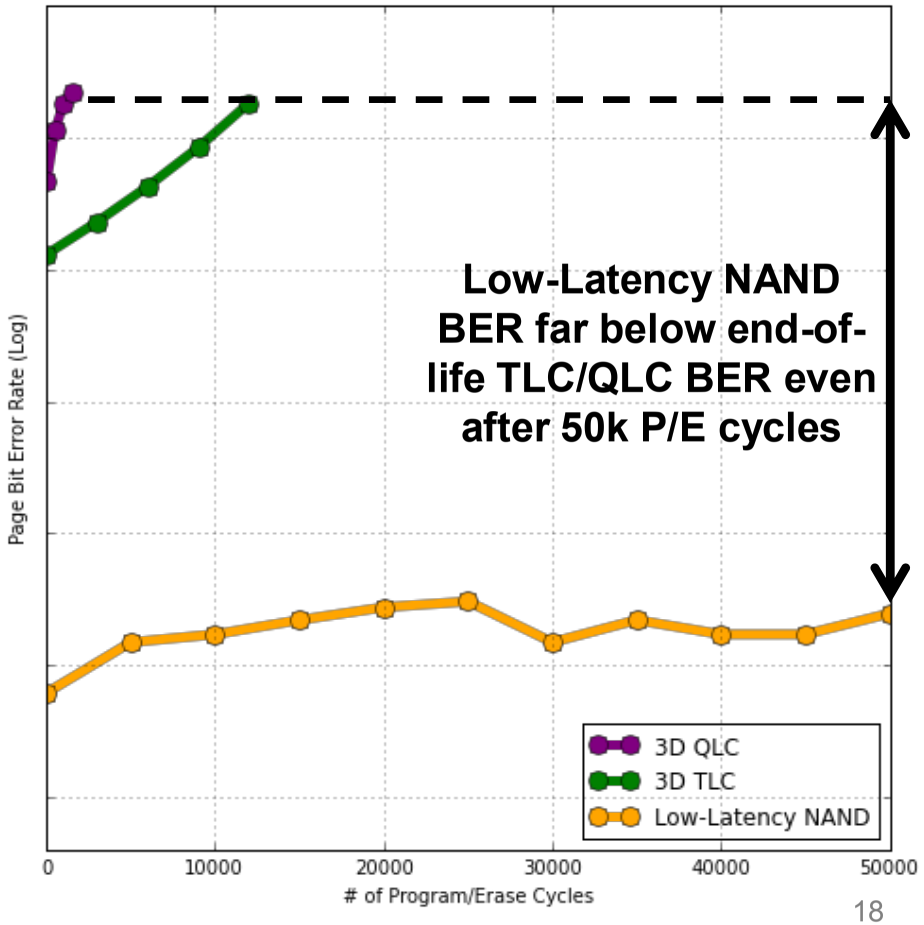
Low-Latency NAND Supports Fast Reads

- Low-Latency NAND is targeted at read-intensive applications where read latency is key
  - Data persistence provides additional advantage over traditional DRAM
- Read latency must be extensively characterized
  - Characterization should ensure read latency can be guaranteed under all expected conditions



Low-Latency NAND Shows Very High Endurance

- Low-Latency NAND shows extremely high endurance
  - Cycling endurance >50k cycles
- High endurance is great for intended application, but poses challenge for testing: characterization takes forever!
  - If characterization cycling is too rapid, results not representative
    - Characterization can be accelerated using mixed-dwell time cycling



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Overall Summary

- 3 Major Cell Types for 3D NAND
  - Triple-Level Cell (**3D TLC**), Quadruple-Level Cell (**3D QLC**), **Low-Latency NAND** (3D SLC)
- Each has unique product applications
- Each presents challenges for characterization
  - Characterization must be well-matched to intended use-case
  - Characterization must account for peculiarities of the technology