Flash Memory Summit

Weebitnano
The Future Memory

Making SiOx ReRAM, a Cost-effective Embedded Memory

Amir Regev

CTO

Flash Memory Summit 2019
Santa Clara, CA

Outline

- **Weebit overview**
- Market opportunities
- Challenges and solutions in ReRAM development
- Conclusions

Weebit LEADERSHIP TEAM

CEO

Coby Hanoch

40 years of experience in the semiconductor industry

CEO of PacketLight

CHAIRMAN

David Perlmutter

Ex-Intel EVP
IEEE Fellow

Brought to Market: Centrino™ mobile technology

EXECUTIVE DIRECTOR

Dr. Yoav Nissan-Cohen

CEO of Tower semiconductors

Co-founder of Saifun Semiconductor

CTO

Amir Regev

45nm NOR Flash Technology Development at Micron

Was part of Intel's Automotive division

DIRECTOR

Atiq Raza

Chairman and CEO of NextGen Inc

President, COO of AMD

ReRAM Market Opportunities

Analog

Replacing EEPROMS

Key Applications:
All types of sensors, PMIC, LED drivers, Audio

Uses:
Trimming
Data storage
Code Storage

Capacities:
64bits – 1/2Mb

IoT

Replacing NOR Flash

Key Applications:
Wearables, security, smart cities

Uses:
Data storage
Code Storage

Capacities:
16Kb –1Mb

Artificial Intelligence

Replacing DRAM usage

Key Applications:
Facial & object recognition

Uses:
Inference
Learning tasks

Capacities:
Mb-Gb

ReRAM usage

For Memory

- Integrated in the back-end metal layers
- Power efficient
- Extremely scalable
- Byte alterable

For AI

- Combines storage and computation
- Promising for analog computing
- Robust and even utilize noise
- Power efficient, dense, non-volatile

Potential game-changer in a wide range of applications

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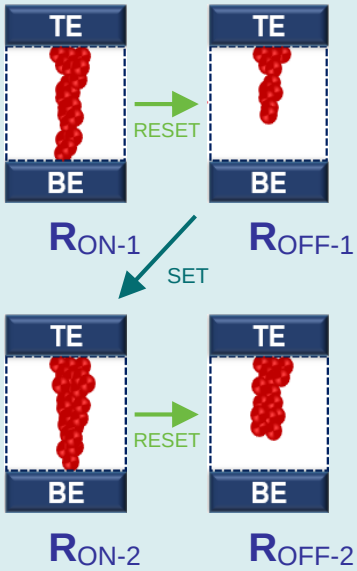
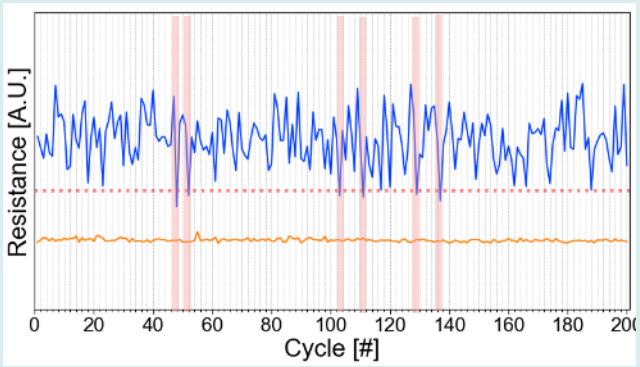
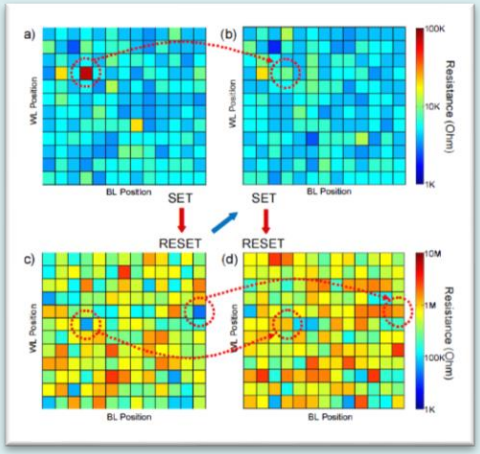
Intrinsic variability

Cycle to Cycle the filament formation is a little different
Gap length and defects distribution in the gap varies
Leads to variability in the resistive states



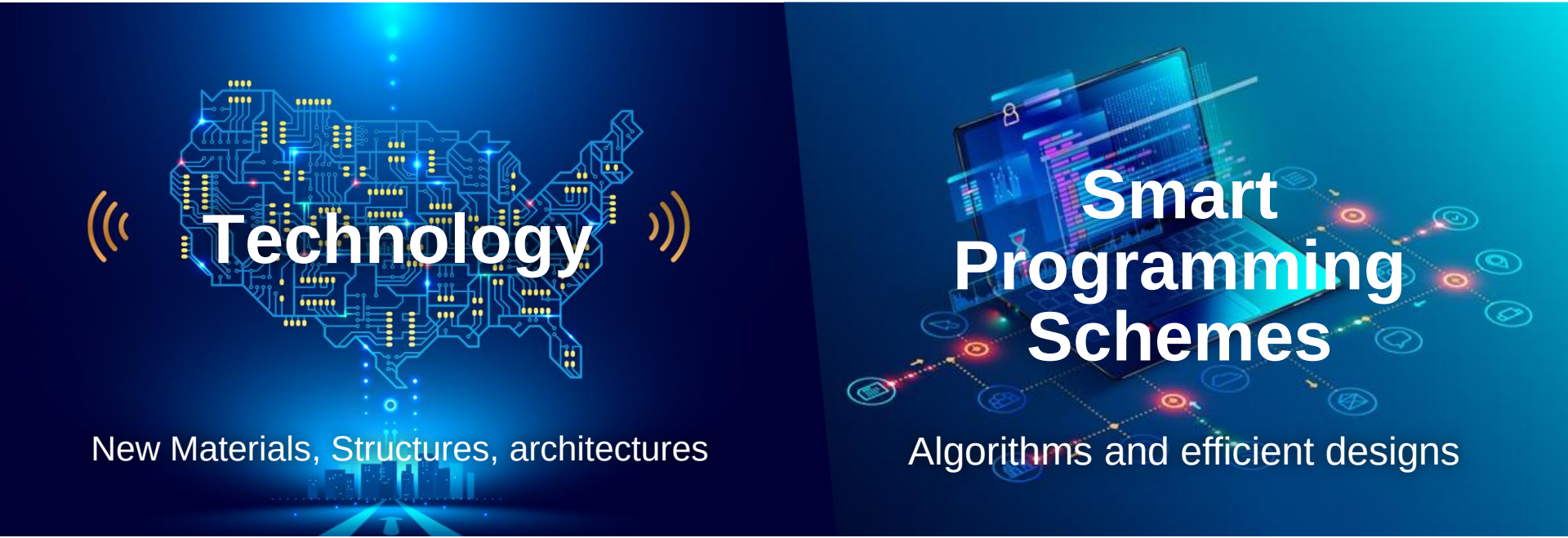
G. Molas, *ECM Aimes 2018*





M.-H. Lee, *IEEE ICSICT 2016*

How to solve variability issues

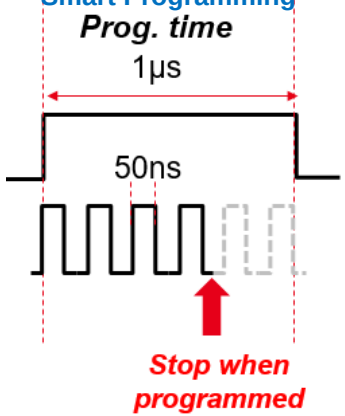


Variability optimization

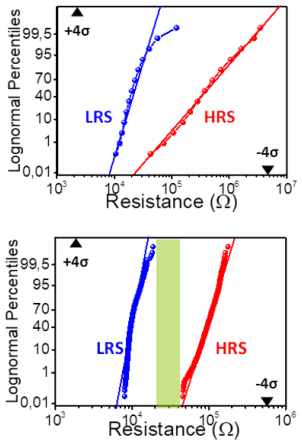
Optimized programming schemes and smart architectures development are key ways to overcome the inherent variability problems:

Smart operation – adaptive forming and programming algorithms:

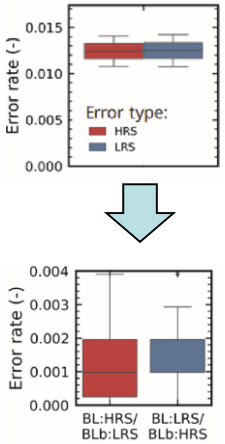
Smart Programming

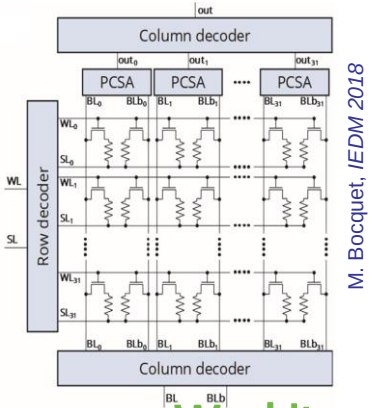


G. Sassine, *IRPS 2018*



Smart architecture





M. Bocquet, *IEDM 2018*

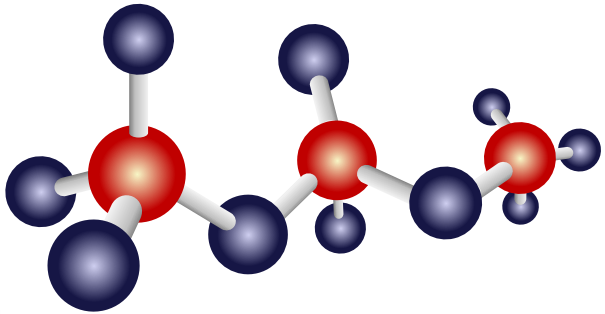
Why Silicon Oxide

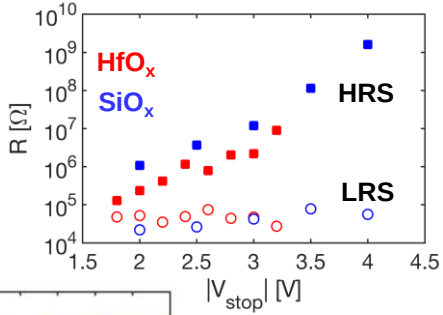
Physical Characteristics

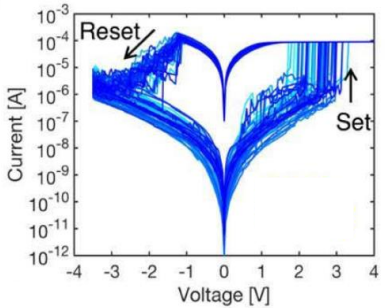
- High bandgap material - large resistive window
- Low leakage
- Low HRS variability
- High temperature stability

Manufacturability characteristics

- Full CMOS compatibility
- High manufacturability
  - Any Fab
  - Any process
  - Any deposition technique
- Easily tunable
  - Thickness
  - Stoichiometry
- Cost effective





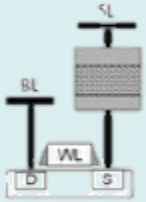


E. Ambrosi, *Faraday Discussions 2019*

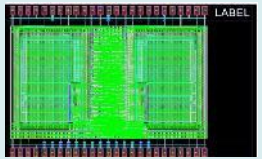
Weebit-Leti Development Partnership

The Weebit-Leti development collaboration is yielding promising results:

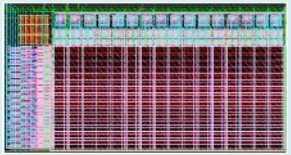
- SiOx ReRAM development kicked of in 2016
- Mbit arrays demonstrated at 40nm memory size
- Continuous improvement of technical parameters



1T-R — 2017

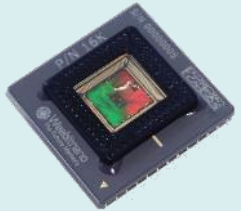


4Kb — Mar 2018



16Kb — May 2018

1Mb — Jun 2018

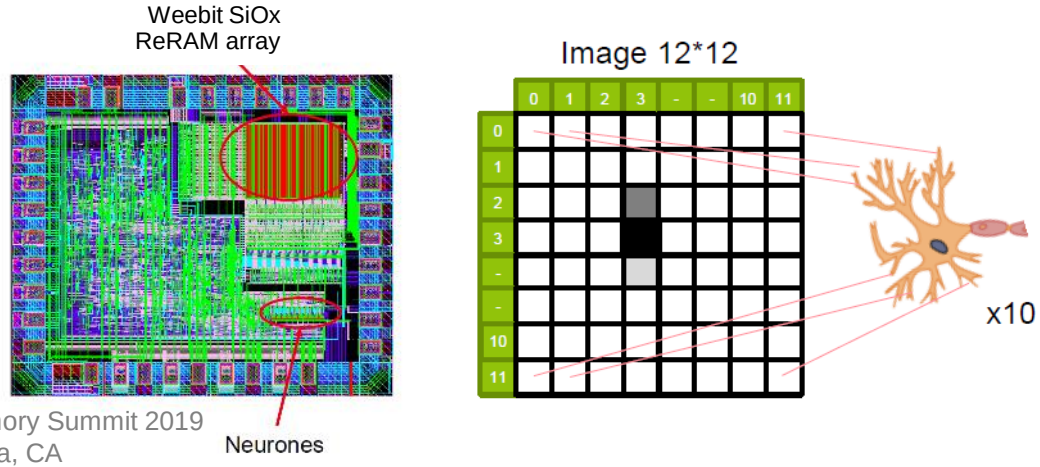


AI Demo — Aug 2019

Weebit-Leti Neuromorphic Demo

- Fully connected Spiking Neural Network combining analog neurons and SiOx ReRAM synapses
- Demonstrating MNIST digits recognition

First fully-integrated SNN using resistive memories as synaptic elements and analog neurons



Hear
my talk on
neuromorphic
computing

Thursday AI/ML
session-301-1

See our live demo
on CEA/Leti booth
#852

THANK YOU

Flash Memory Summit

Weebitnano
The Future Memory