EVERSPIN TECHNOLOGIES

Data Persistence at Speed

STT– MRAM: High Density Persistent Memory Solution

Sanjeev Aggarwal

Safe Harbor Statement

Forward-Looking Statements

This presentation contains "forward-looking statements" that involve risks, uncertainties and assumptions. If the risks or uncertainties materialize or the assumptions prove incorrect, our results may differ materially from those expressed or implied by such forward-looking statements. All statements other than statements of historical fact could be deemed forward-looking statements, including, but not limited to: any estimates of addressable market size and our ability to capture that market, market trends and market opportunities, customer growth, product availability, technology developments, or other future events; any statements about historical results that may suggest future trends for our business; any statements regarding our plans, strategies or objectives with respect to future operations or business performance; any statements regarding future economic conditions; and any statements of assumptions underlying any of the foregoing. These statements are based on estimates and information available to us at the time of this presentation and are not guarantees of future performance. Actual results could differ materially from our current expectations as a result of many factors, including, but not limited to: market adoption of our products; our limited operating history; our ability to raise capital; our history of losses; our rate of growth; our ability to predict customer demand for our existing and future products; our ability to hire, retain and motivate employees; the effects of competition, including price competition; technological, regulatory and legal developments; and developments in the economy and financial markets.

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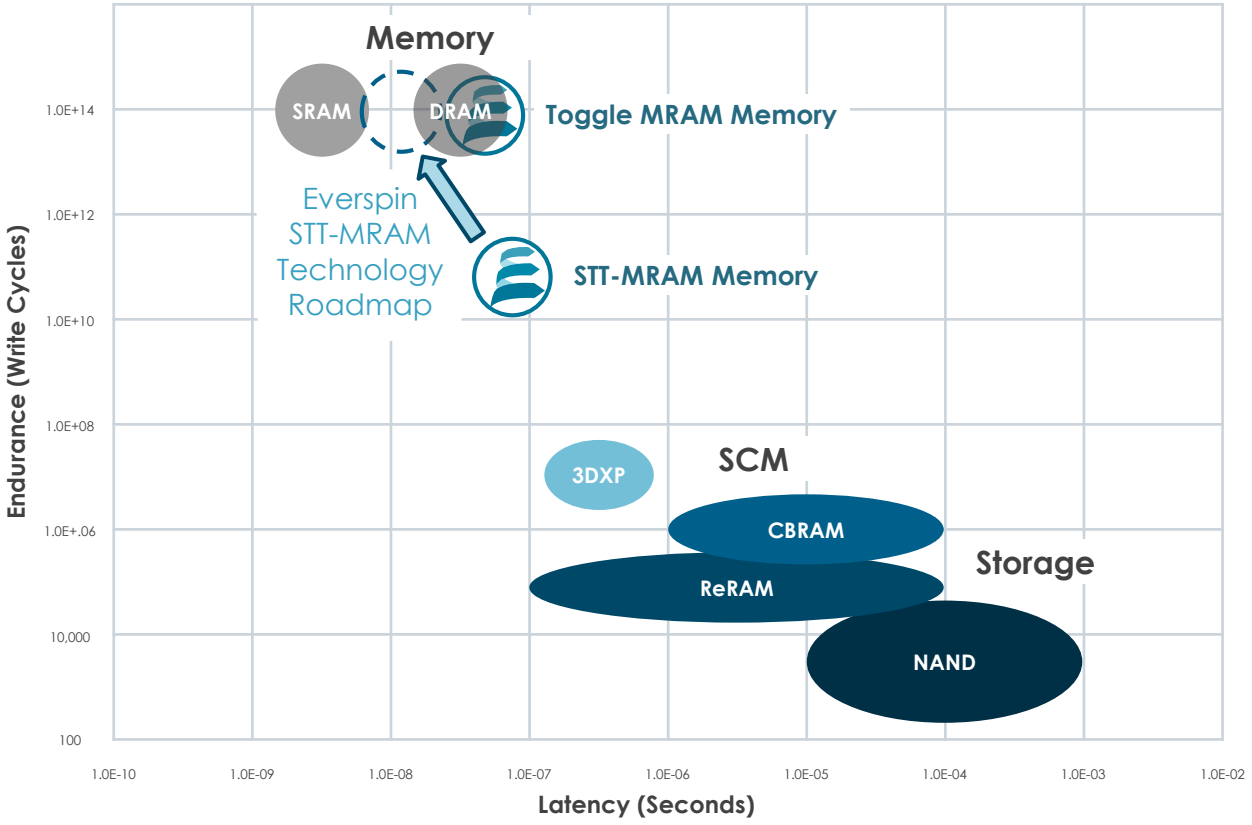
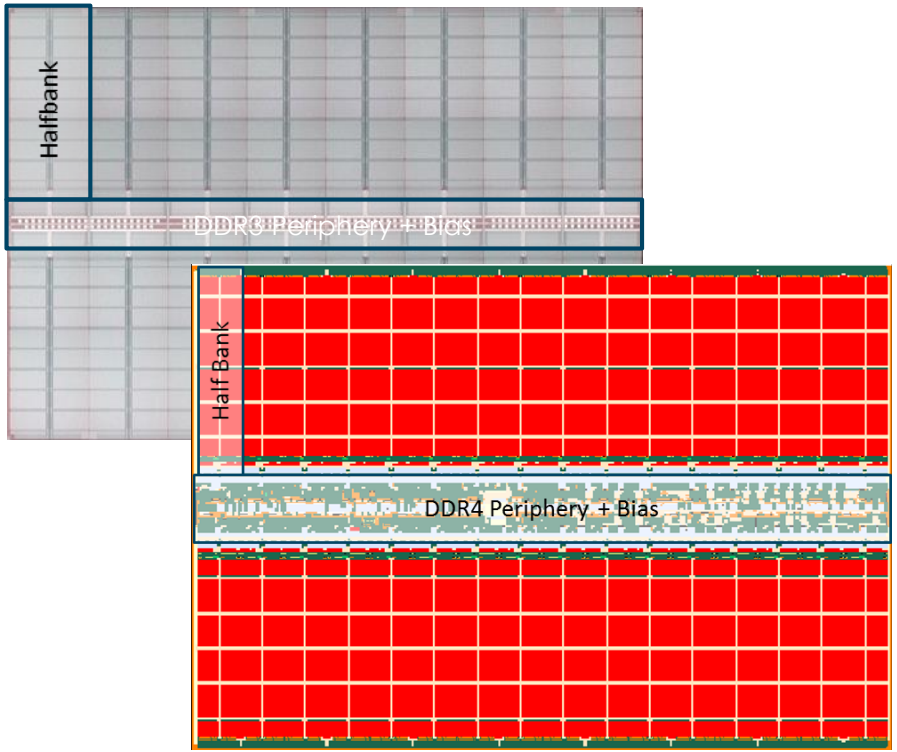
MRAM Brings Native Persistence to Memory Workloads



MRAM COMBINES PERFORMANCE OF MEMORY WITH PERSISTENCE OF STORAGE

- **Non-Volatile:** Maintains data without power or refresh
- **Fast:** Read/write similar to DRAM
- **Endurance:** Handles memory workloads

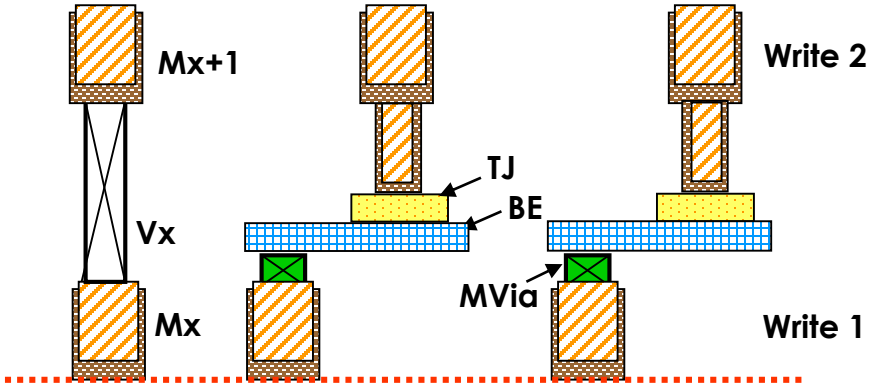
Everspin STT-MRAM in Production



- 256Mb ST-DDR3 MRAM
  - 40nm CMOS
  - 1.5V DDR3 VDD/VDDQ
  - Standard JEDEC DDR3 ball configuration
- 1Gb ST-DDR4 MRAM
  - 28nm CMOS
  - 1.2V standard DDR4 VDD/VDDQ
  - Standard JEDEC DDR4 ball configuration

STT-MRAM – Easy to Integrate with Standard CMOS

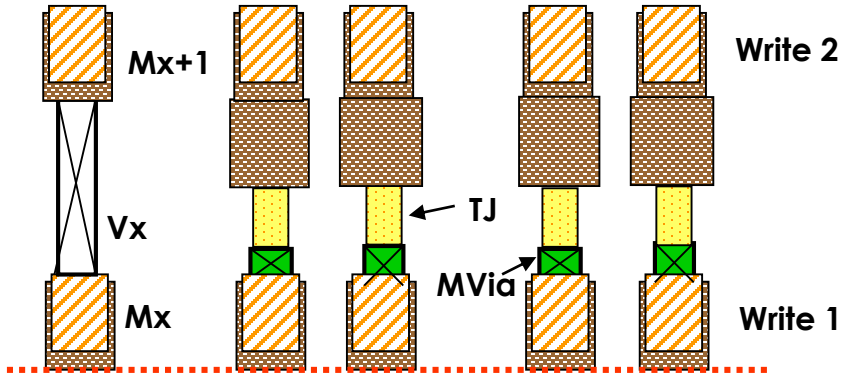
Off Axis Integration, 256Mb



MRAM Layer Additions

MVia	TJ	BE	TJVIA
Msk1	Msk2	Msk3	Msk4

On Axis Integration, 1Gb



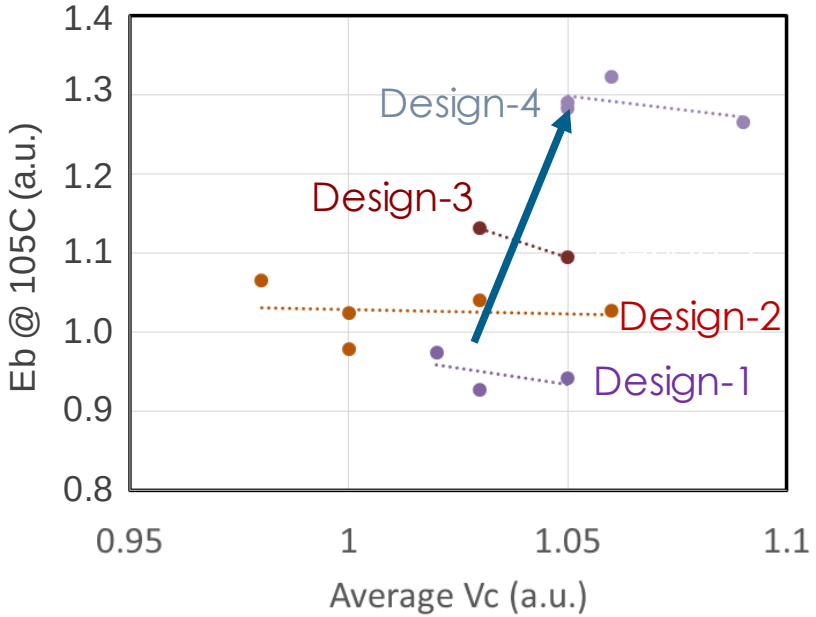
MRAM Layer Additions

MVia	TJ	Trench
Msk1	Msk2	Msk3

Free Layer Engineering for STT Efficiency

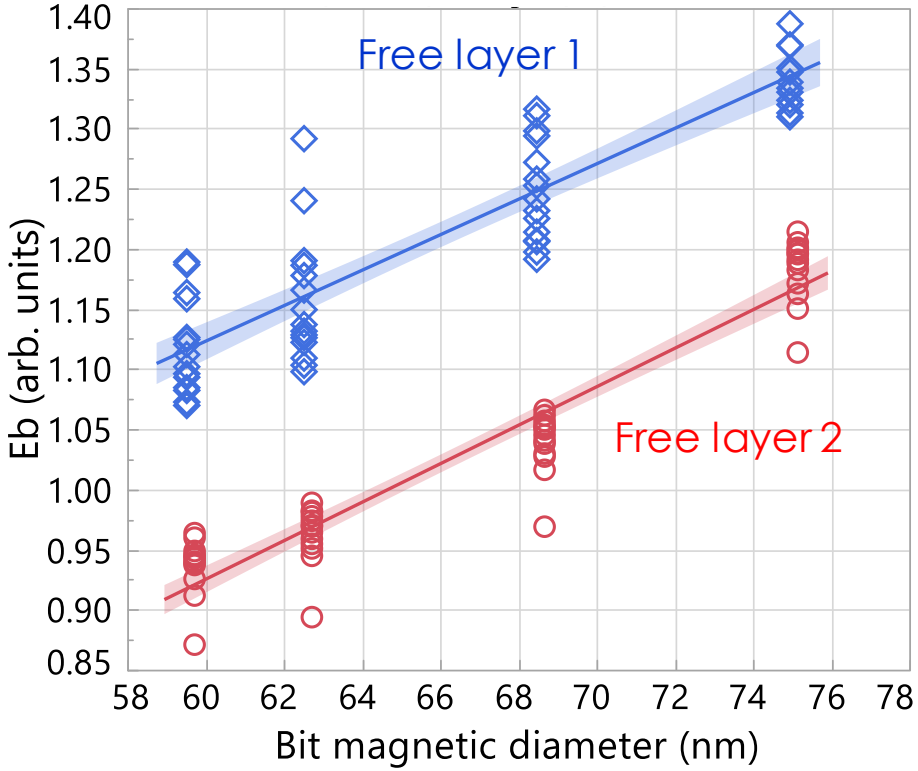
- Free layer designs with different materials
  - Lower Vc and higher Eb indicates better STT switching efficiency
  - Figure of Merit for product efficiency and reliability is:

    Eb(105 C) / Vc(20 C)
- Each series is a range of thickness
- Eb is flat but Vc varies for a range of thickness near the optimum Eb design point
- Eb increased ~35% with <5% increase in Vc from lowest to highest Eb design



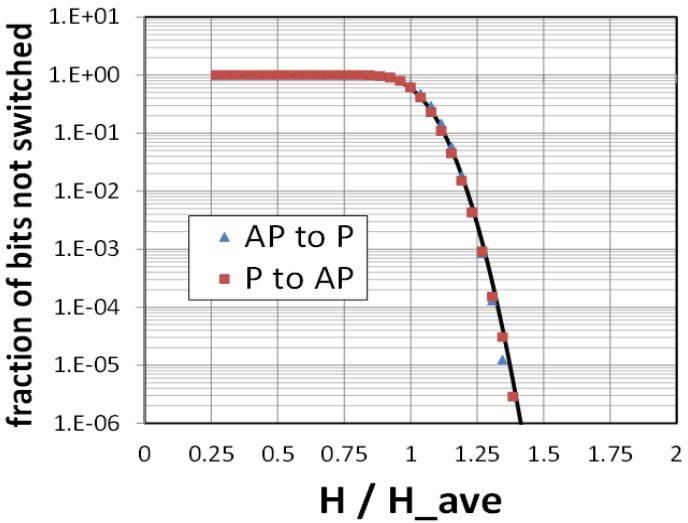
Materials Design for Scaling

- Data retention bakes at 160°C
- Data retention flips measured for 4 nominal bit sizes and fit to obtain Eb
- Eb decreases linearly with bit diameter
- Magnitude of Eb is tunable through free layer design

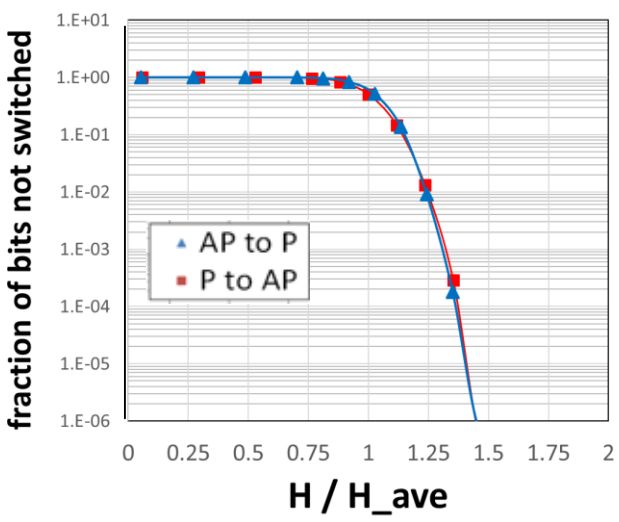


Reliable Switching with Narrow Distributions

256Mb DDR3 STT-MRAM



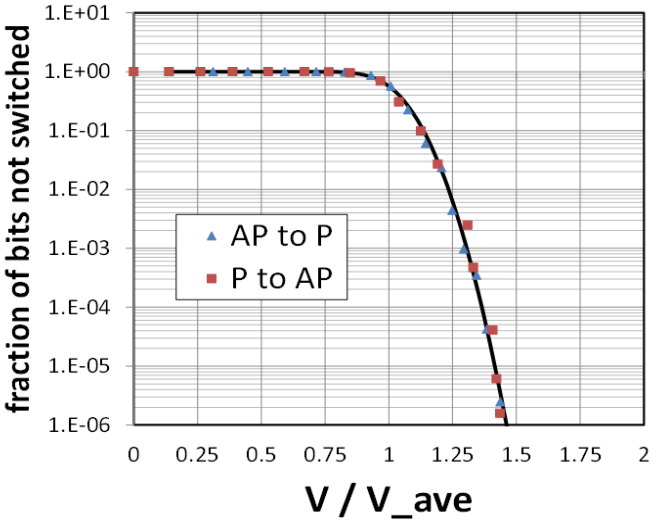
1Gb DDR4 STT-MRAM



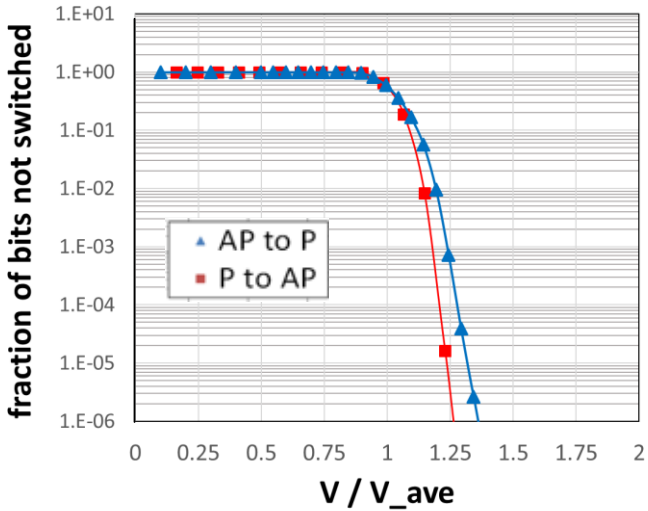
- The field switching distribution correlates to the resistance to thermal fluctuation
- The large separation from 0 field indicates essentially zero probability of spontaneous flips

Better Margin for Manufacturability

256Mb DDR3 STT-MRAM



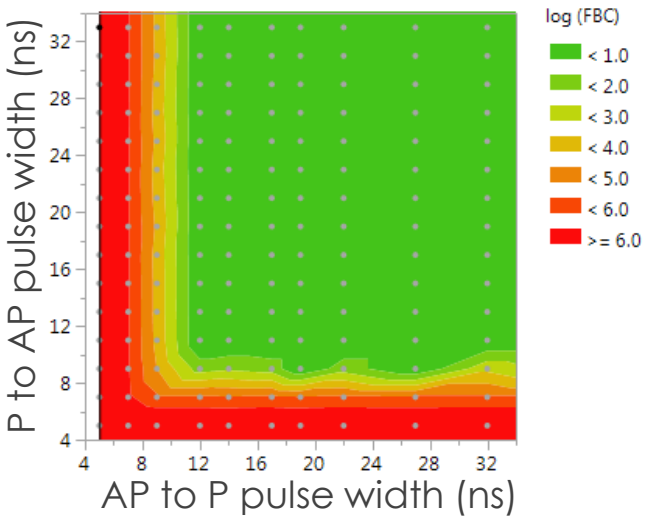
1Gb DDR4 STT-MRAM



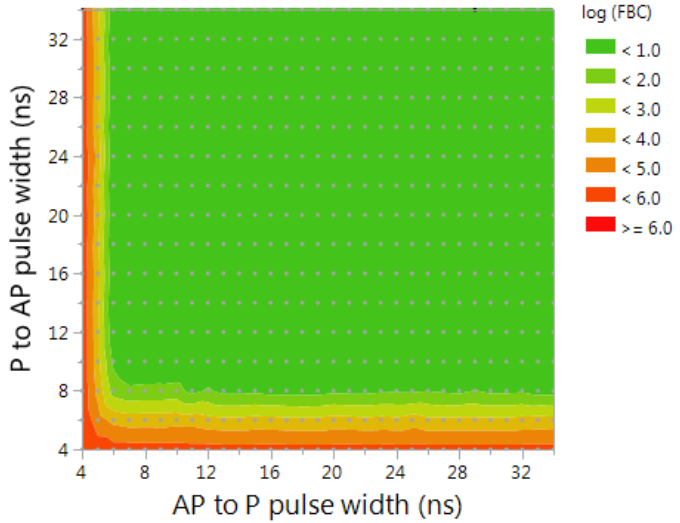
- Error rates < 1E-6 (raw bit error rate) achieved for both 256Mb and 1Gb
  - Relative Vswitch of > 1.5 for 256Mb and > 1.4 for 1Gb
  - Improved (narrower) distribution in both directions going from 256Mb to 1Gb

Improving Switching Efficiency

256Mb DDR3 STT-MRAM



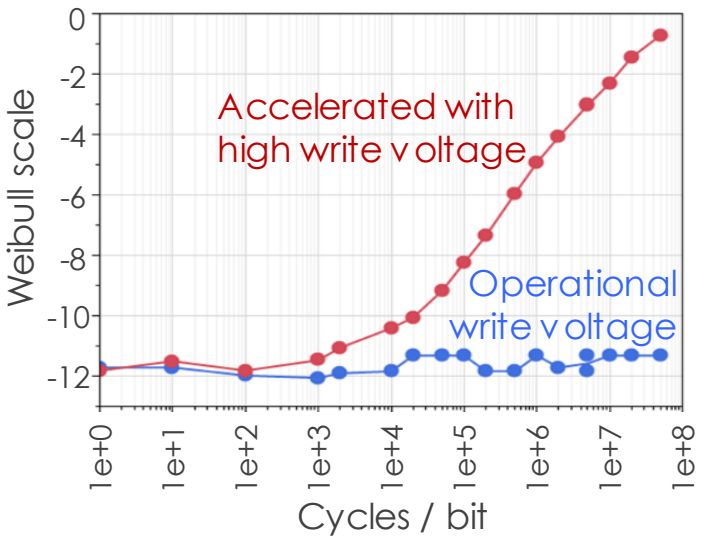
1Gb DDR4 STT-MRAM



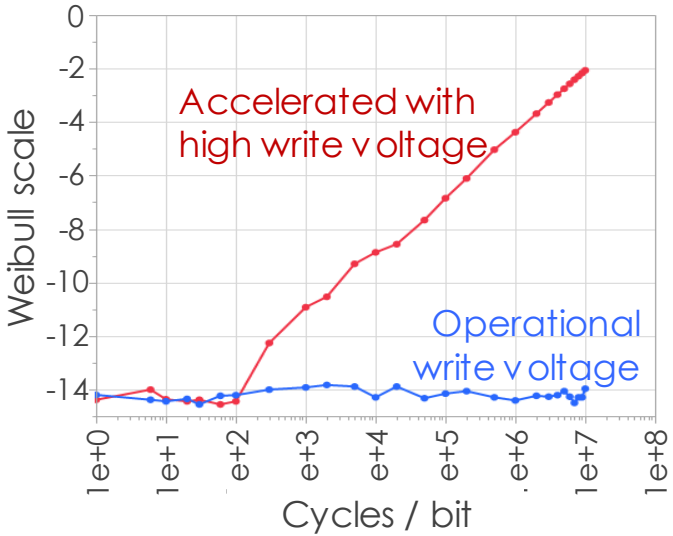
- Zero fails for range of write pulse widths ≥ 10-12 ns for 256Mb and ≥ 6-8 ns for 1Gb
  - Endurance is better with longer pulses due to the lower required write bias
  - Clock rate is not affected by the choice of pulse width in this range
- Improved switching efficiency for 1Gb enables better performance

Reduction in Extrinsic for Better BER

256Mb DDR3 STT-MRAM



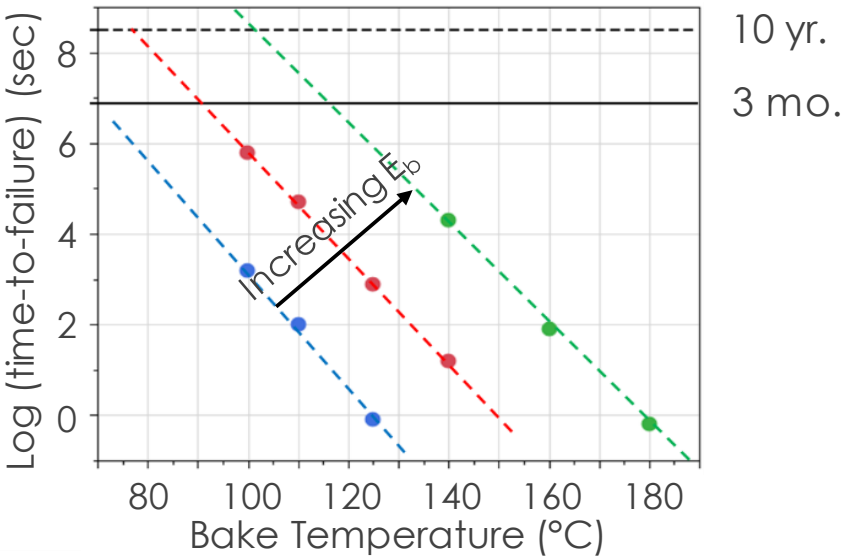
1Gb DDR4 STT-MRAM



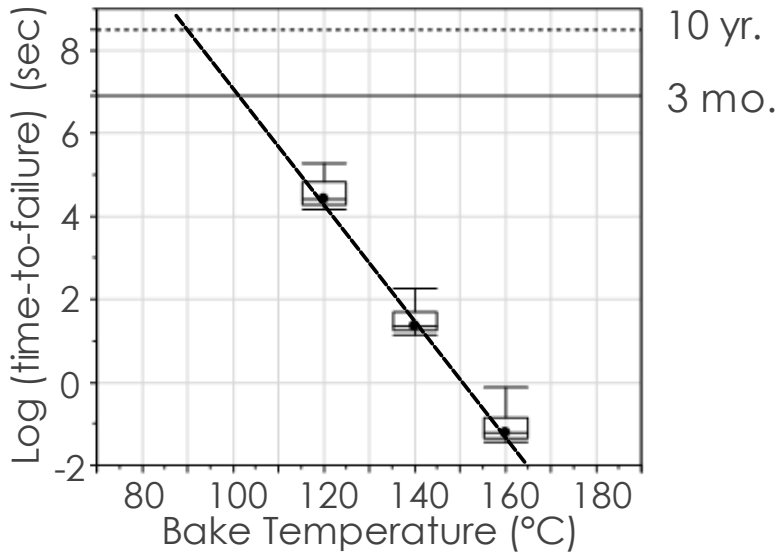
- Full array cycling with stress to accelerate fails
  - Used bias and temperature acceleration to predict endurance at operating conditions
  - Product endurance >1E10 cycles to BER specification is demonstrated
- Improved extrinsics for 1Gb (linear down to -14 on Weibull scale)

Widening Operating Temperature Range

256Mb DDR3 STT-MRAM

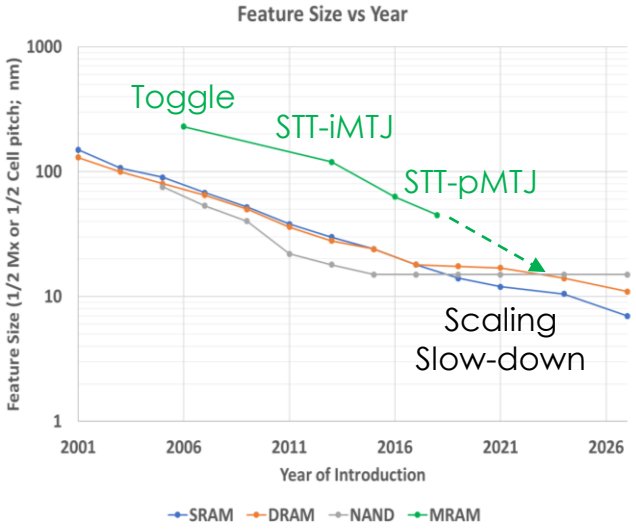


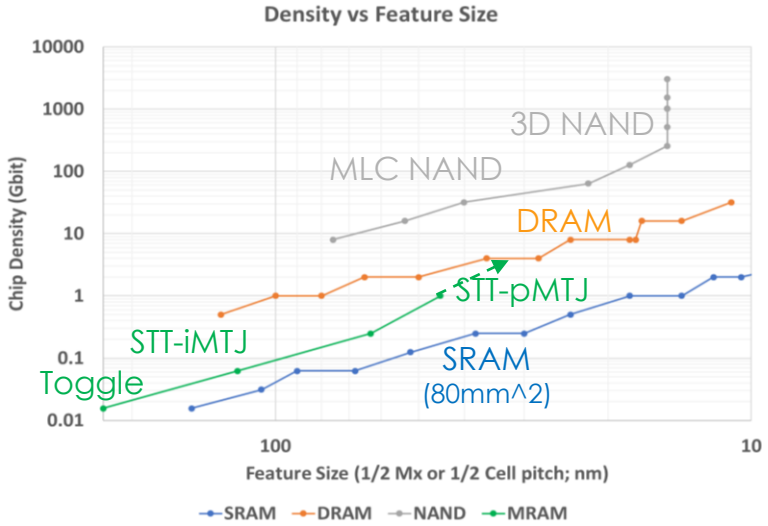
1Gb DDR4 STT-MRAM



- Baked parts at elevated temperature to accelerate fails
  - Free layers engineered to achieve desired data retention
- 10yr @ 85C data retention achieved for 1Gb parts with 1e10 endurance

The STT-MRAM Revolution has Started





- Everspin has successfully transitioned STT-MRAM from R&D to volume manufacturing
- STT-MRAM is approaching DRAM Density and Feature Size
  - Switching efficiency improvements for STT-MRAM expected to scale with bit size enabling

Source for SRAM, DRAM, NAND:
The International Technology Roadmap for Semiconductors
The International Roadmap for Devices and Systems

Acknowledgements

- Colleagues at Everspin Technologies:
  - H. Almasi, M. DeHerrera, B. Hughes, L. Hui, S. Ikegawa, J. Janesky, H. K. Lee, F.B. Mancoff, K. Nagel, G. Shimon, J.J. Sun, T. Andre, S. M. Alam

- Partners for STT-MRAM Manufacturing & Development

Thank you.

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