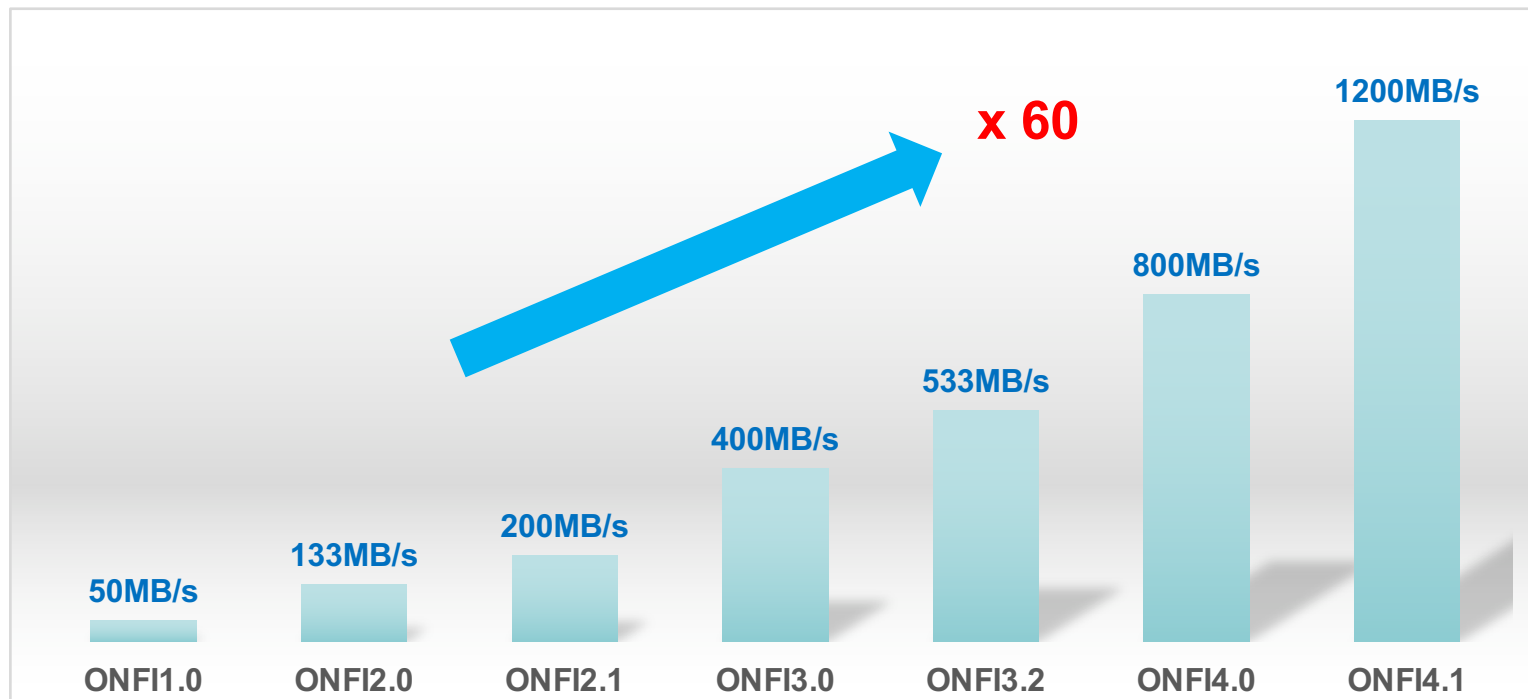




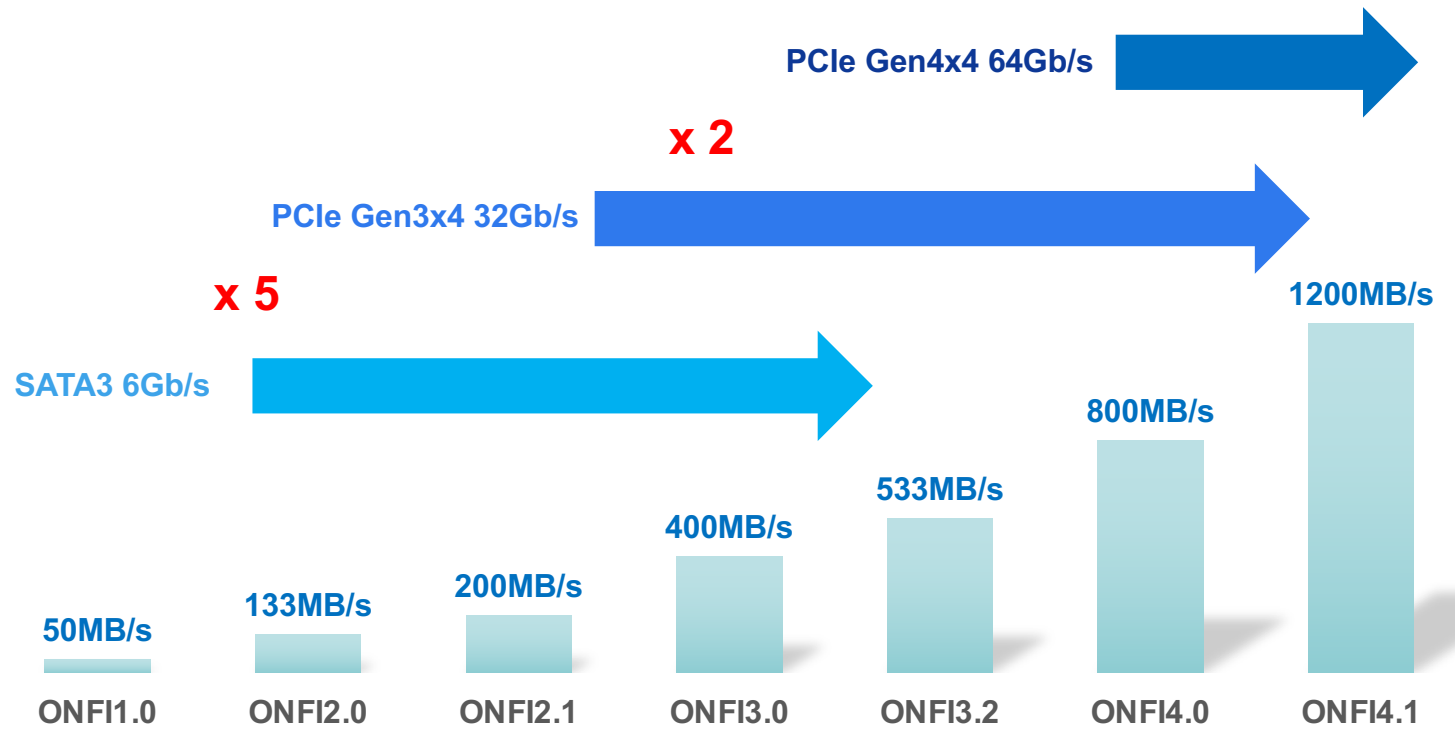
A HW/FW Co-Designed SSD Controller Architecture to Boost up SSD Performance

Wei Xu
August 8, 2019

Explosive NAND IF Bandwidth

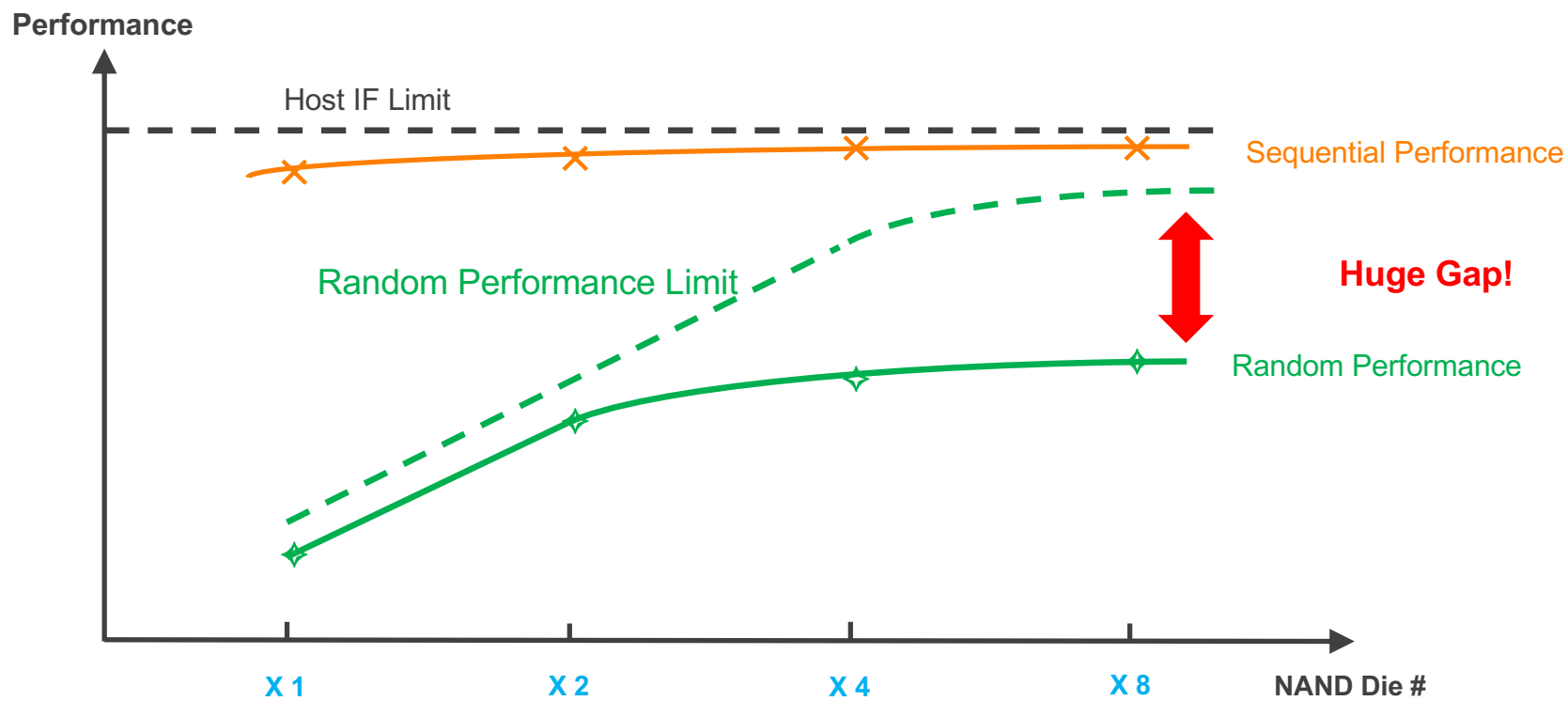


Client SSD Trend

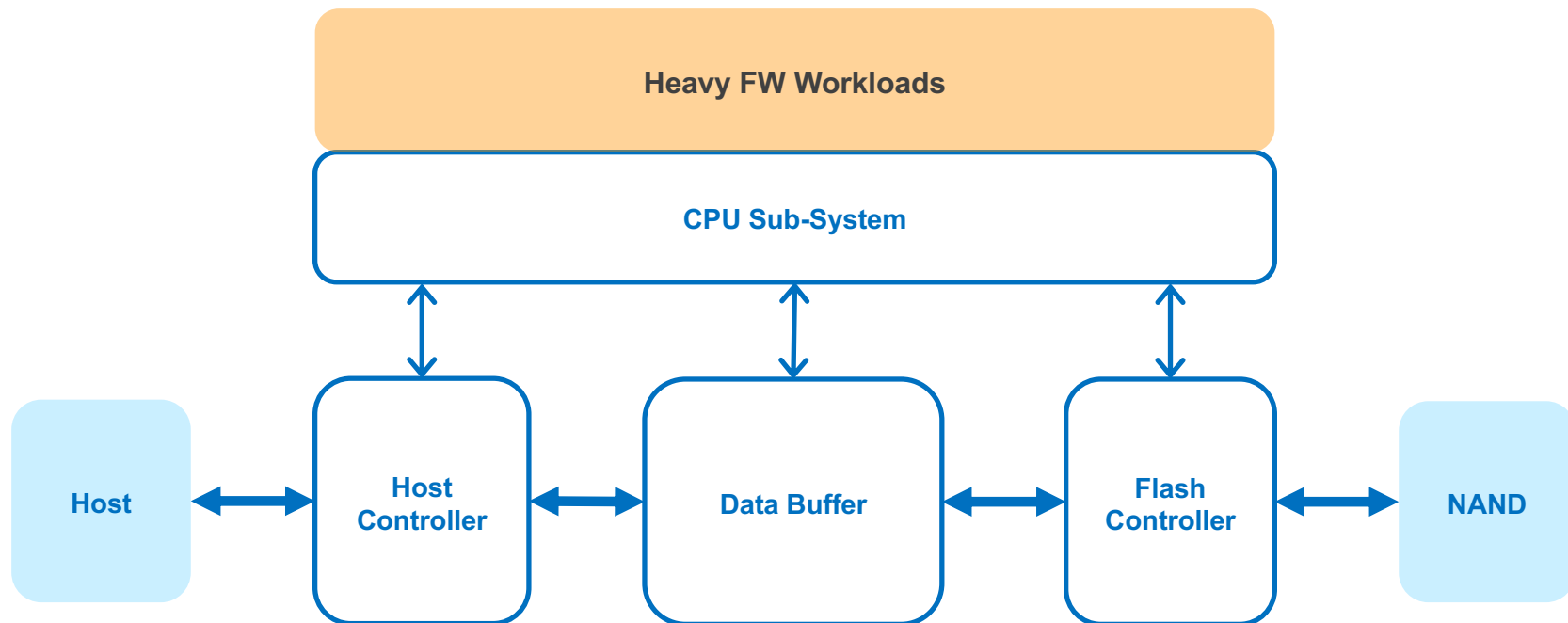




SSD Performance Issue

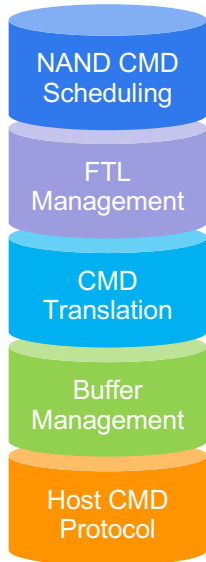


Bottleneck of SSD Performance

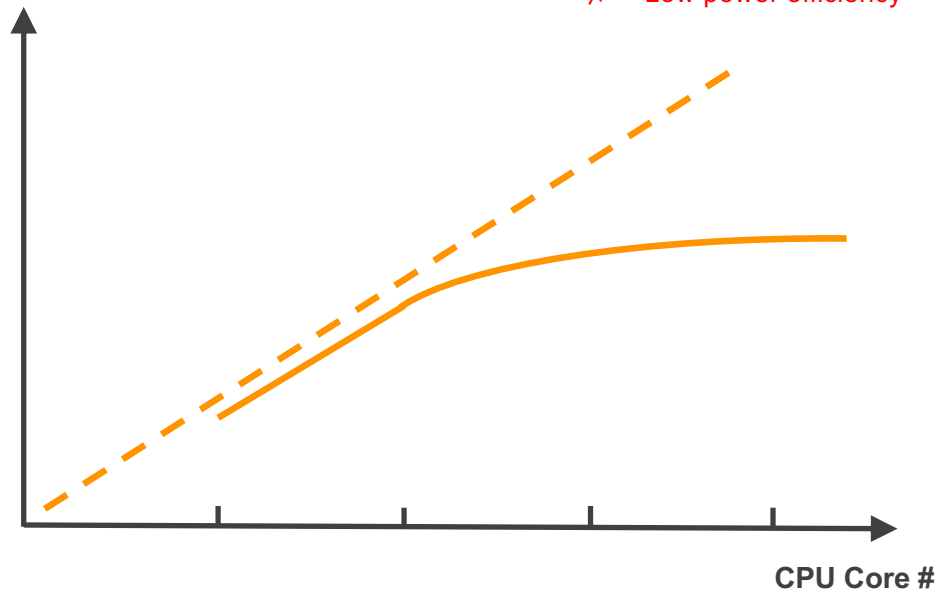


Details of CPU Workloads

Heavy CPU workload

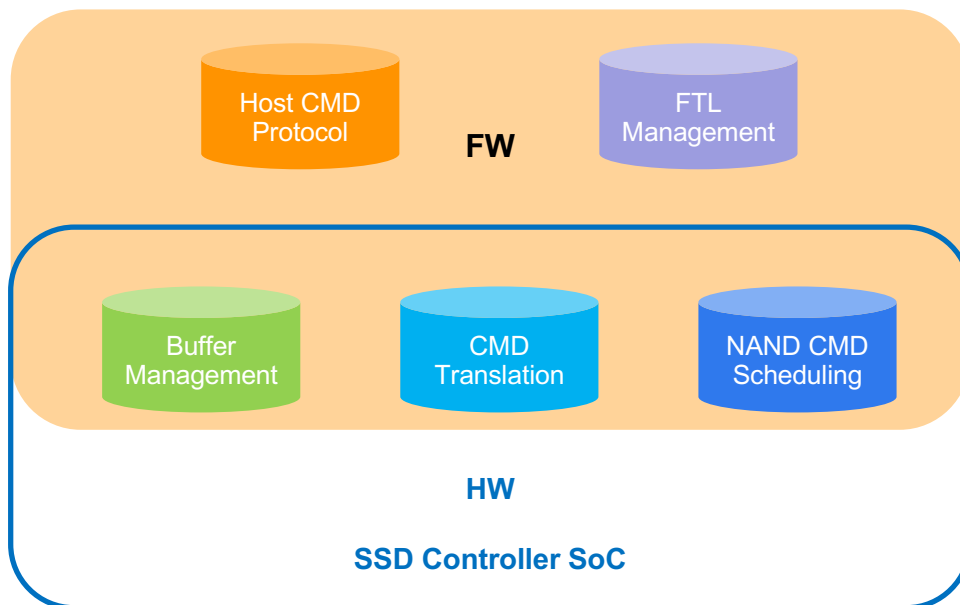


SSD Performance



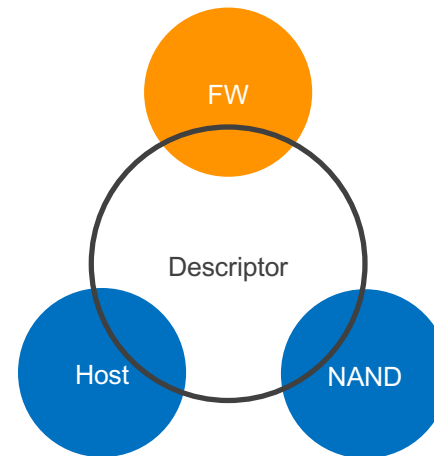
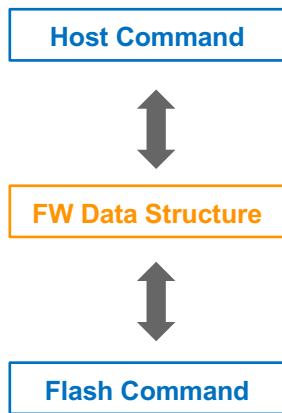
- Typical solution: Increasing CPU cores
 - X More CPU partitions
 - X Complicated FW architecture
 - X Low power efficiency

Cross-Layer Design Methodology



- ❑ HW/FW Co-designed architecture to offload CPU
 - ✓ Seamless FW/HW flow
 - ✓ Simple FW architecture
 - ✓ High power-efficient

Unified HW/FW Data Structure

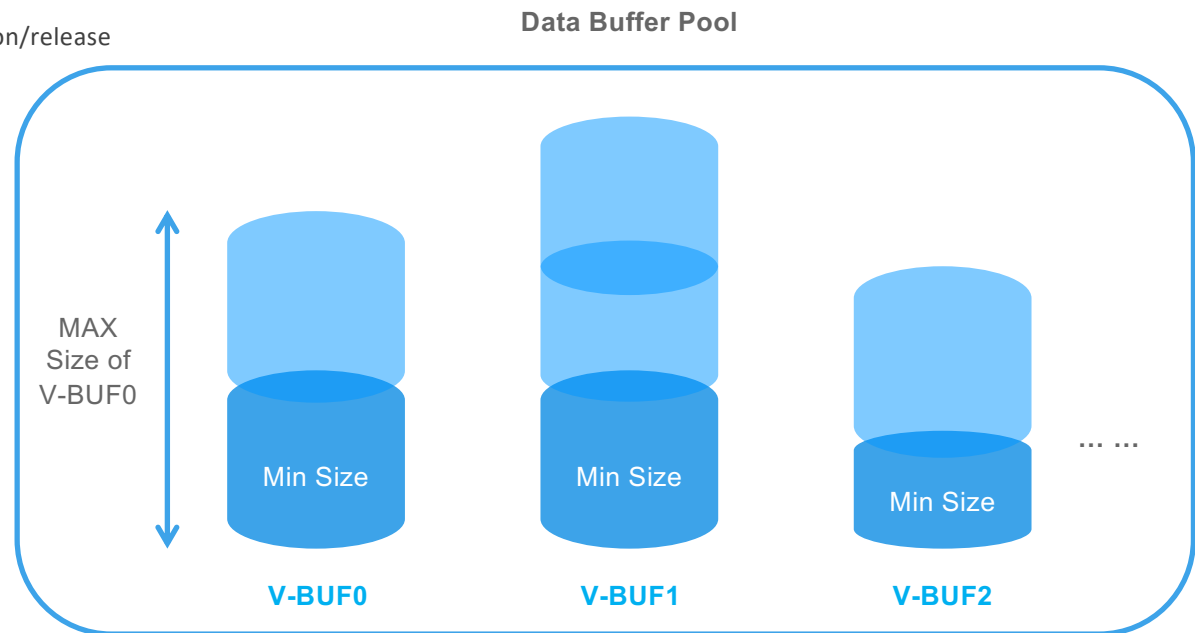


- ❑ HW/FW Shared data structure (e.g., descriptor), containing all information about the atomic data unit managed by FW.
- ❑ HW automation for descriptor pool management, including descriptor allocation/release and queue management.

Virtual Buffer Management

- ❑ Physical buffer segments shared by virtual buffers
 - ✓ Virtual buffers are defined by FW
 - ✓ HW automation of buffer allocation/release

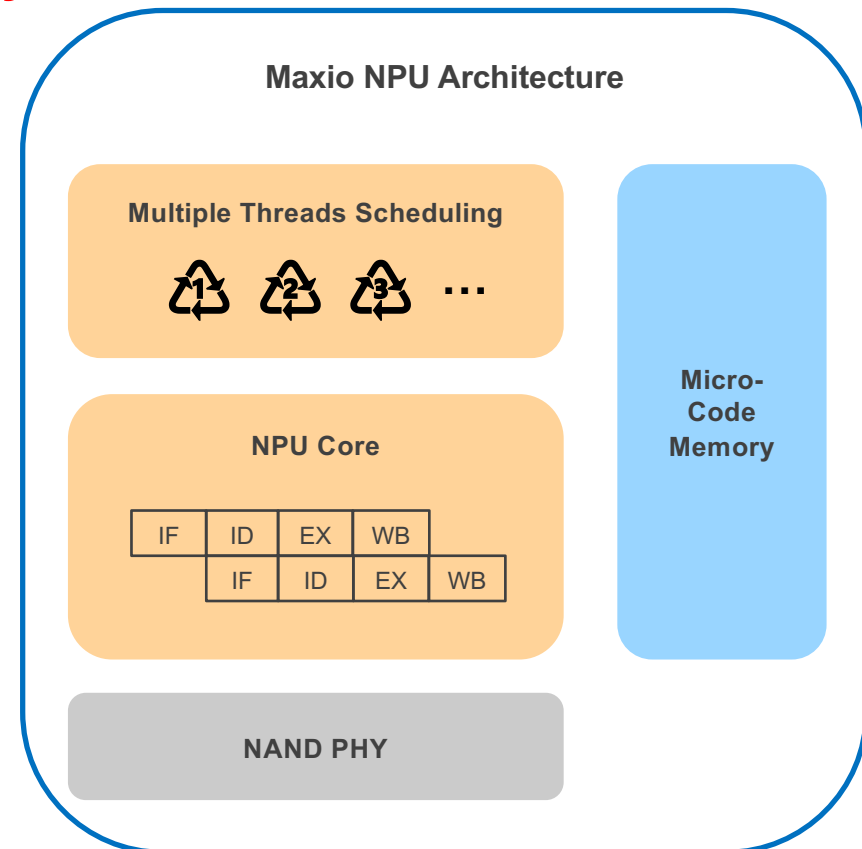
- ❑ Virtual buffer attributes
 - ✓ Buffer ID
 - ✓ Min/max size
 - ✓ Buffer allocation policy



Maxio NPU Technology

- ❑ Private instruction set for NAND flash memory
 - ✓ Flexible NAND command sequence
 - ✓ Support NAND models of all NAND vendors

- ❑ Specified NAND Processing Unit (NPU) architecture - NPU
 - ✓ Support multiple thread
 - ✓ HW automation of thread interleaving
 - ✓ NPU core: 4 pipeline stages for high speed NAND IF

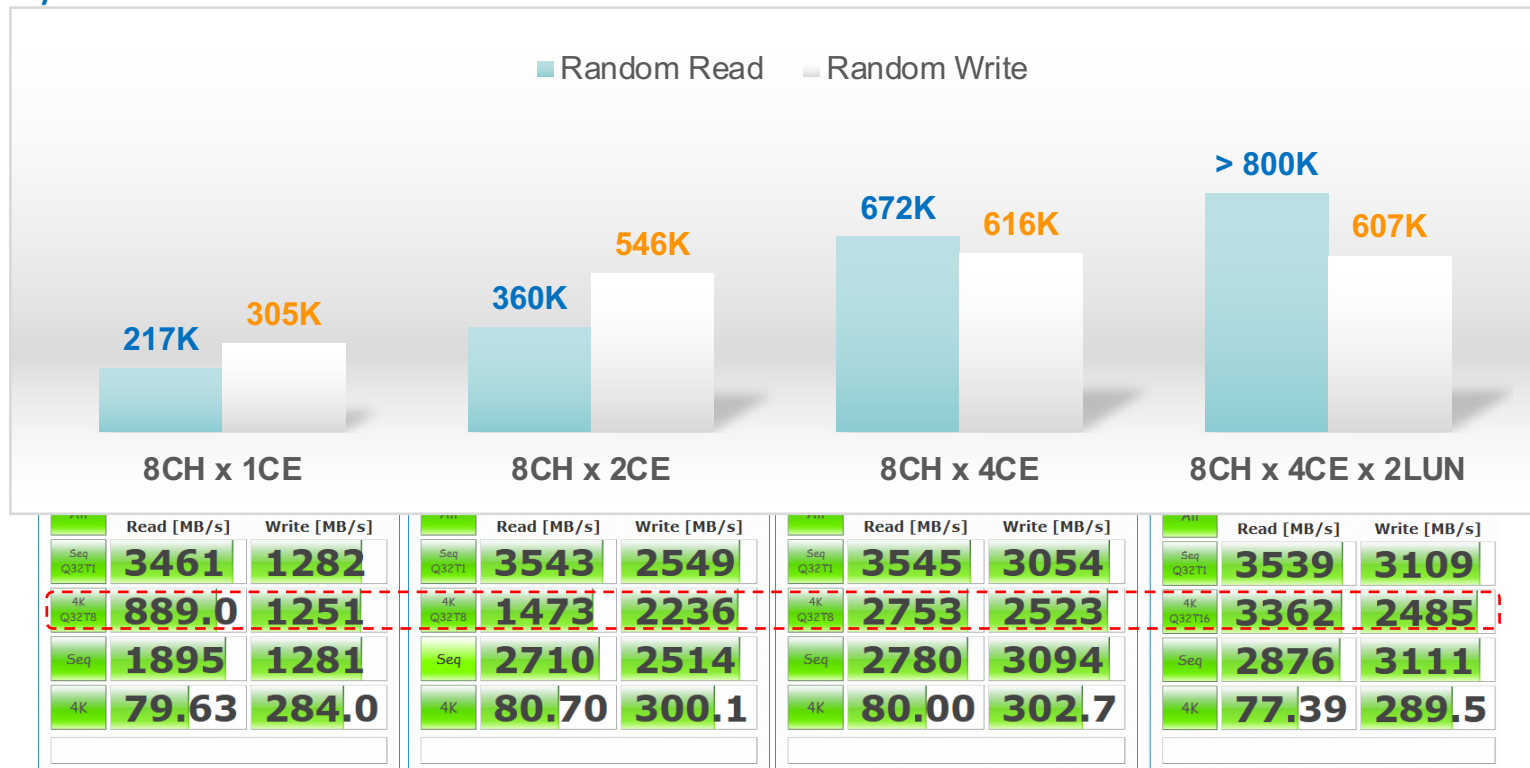




Flash Memory Summit



Maxio MAP1001 Performance Result





Flash Memory Summit

Maxio Technology



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