

## Benefits and Use Cases for NVMe-oF SmartNICs

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Flash Memory Summit 2019 Santa Clara, CA



## Why a SmartNIC

### Moore's Law diminishing returns

- Vertical scaling power & cost model no longer viable

### CPU costs increasing

Economic benefits to limiting core count

## Multi-socket interconnect bottleneck

- I/O, memory transactions across interfaces add latency
- 2<sup>nd</sup> socket often used to get more memory and I/O
- TCO penalty for 2<sup>nd</sup> socket
- Distributed cloud architecture
  - Smaller fault domains



Original data up tot the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batter New plot and data collected for 2010 - 2017 by K. Rupp



3yr server & 10yr infrastructure amortization

Source: James Hamilton, AWS



#### Architectural flexibility to quickly offload multiple overhead laaS services





## **Evolution of SmartNIC...**

## FPGA + NIC

...........

#### Pros

- Typical single function offload
- Good performance

#### Cons

- Hard to design for performance
- Slow feature velocity (RTL)
- High power
- · Large devices are expensive

#### Network Function Processor



#### Pros

 More than single function

#### Cons

- Non-standard programming
- Can be expensive
- High power

#### Pros

- Performance/Watt
- General-purpose with standard programming
- Great feature velocity

#### Cons

 Performance varies based on CPUs, DDR, and availability of integrated accelerators

#### HFT, HPC, Telco I/O

#### Telco I/O

#### **Cloud DC & Telco**

## Flosh Memory Summit Platform Economics: CPU Workload Partitioning



#### Only 8-12 Cores Available for Applications

Services can consume most the remaining cores

# Flosh Memory Summit Platform Economics: SmartNIC Workload Partitioning



Offloading services to SmartNICs frees up cores for applications



## **SmartNIC Storage Use Cases**



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÷ NVMe-oF™

#### **Test Summary**

Parameter	4x Stingray Targets	2 Socket-x86 Target
Network Link	4x 25G	1x 100G
NVMe SSDs (x2 Gen3)	32	30
4K Random Read	2.0M IOPS 🍟	1.8M IOPS
512K Sequential Write	37K IOPS 🍟	18K IOPS
<b>Tail Latency</b> (mean – P90% – P99.9%)	2 ms – 6.2 ms – 11 ms 🝟	2.3 ms – 12.9 ms – 23.5 ms
CPU+DRAM Power (estimated)	160W 🍟	300W



#### **SmartNIC Disaggregated Storage Advantages**

- Better performance
- Lower power
- Smaller fault domain reduces blast radius exposure (16TB vs 60TB)

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# SmartNIC in NVMe-oF<sup>™</sup> – We Have Come A Long Way but...





- Limited to recent versions of Linux
- No announced support for other operating systems



SO



University of New Hampshire InterOperability Laboratory



NVMe/TCP™ Ratified Nov 2018

Ecosystem is maturing but broad adoption requires solution to OS support problem

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Introducing **Glass Creek** 

## **Applications**

- Storage disaggregation for any OS
- Works with standard NMVe drivers
- Storage virtualization
  - Bare metal and virtualized servers
- Storage services offload
  - Logical Volume Management
  - RAID/EC, De-dupe, Crypto

Flash Memory Summit



## Summary

## Why SmartNIC

- System architecture, cost and performance
- Dual socket architectures are inefficient
- End of Moore's Law

## Market adoption of SmartNIC

- Highly programmable
- CPU-based
- More flexible architecture

## Use cases

- Offloading storage and networking services
- Software-defined storage
- Security

## Expanding ecosystem

- Multiple vendor support
- NVMe-oF and new NVMe virtualization